cas 1909 EP

D1

(12) UK Patent Application (19) GB (11) 2 100 890 A

(21) Application No 8120369
(22) Date of filing 1 Jul 1981
(43) Application published 6 Jan 1983
(51) INT CL³ G04C 11/04
(52) Domestic classification G3T AAF DD JA KA KB
(56) Documents cited
GB A 2017357
GB A 1574758
GB 1424857
GB 1158368
GB 1041859
GB 0993022
GB 0837165
US 4020628
(58) Field of search G3T
(71) Applicant
Chu Tsan-Chen,
31—2 Alley 5,
Lane 100,
Tun Hua S Road,
Taipei City,
Taiwan
(72) Inventor
Chu Tsan-Chen
(74) Agents
Marks and Clerk,
57—60 Lincoln's Inn Fields,
London,
WC2A 3LS

(54) Automatic correction of electronic timepiece

(57) A timepiece (106) comprises means (108,111) for periodically and automatically connecting the timepiece (106) to a standard time signal via a telephone system (40,45,46) and means (109,110,112,113) for automatically synchronising the timepiece (106) with the standard time signal. The timepiece (106) is preferably capable of automatically adjusting its frequency or running speed in accordance with the deviation from the standard time, thus minimising accumulative errors between synchronisations.

The telephone standard time signal may be derived from the generally available vocal time repeat or "talking clock". In this case, the time signal may be identified from the vocal signal by differences in period between subsequent signals and the time signal may be further identified by counting the number of vocal signals associated with it.

The timepiece (106) may be connected to several secondary timepieces (107) of simpler construction, for example not having the automatic telephone communication facility, in order to provide a system of synchronised timepieces.

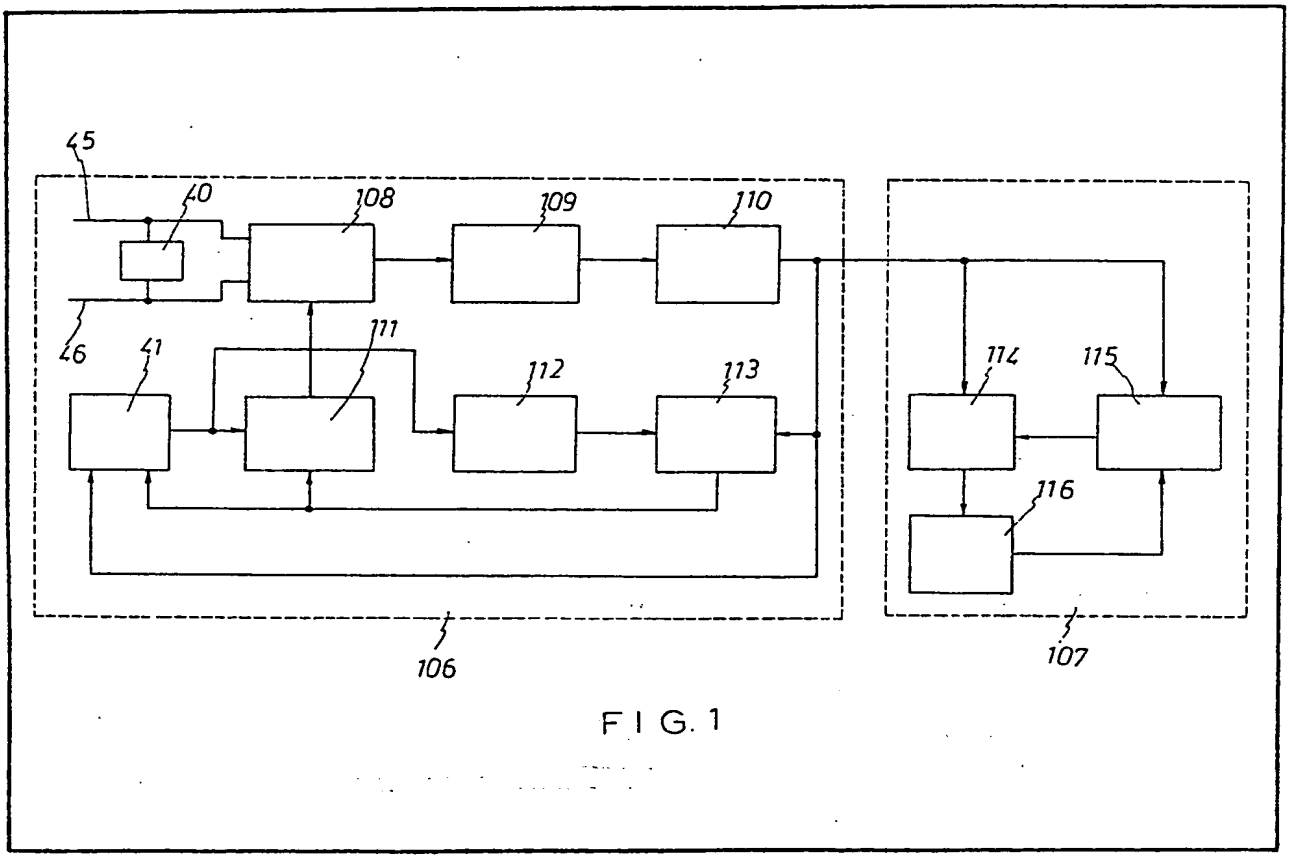


FIG. 1

GB 2 100 890 A

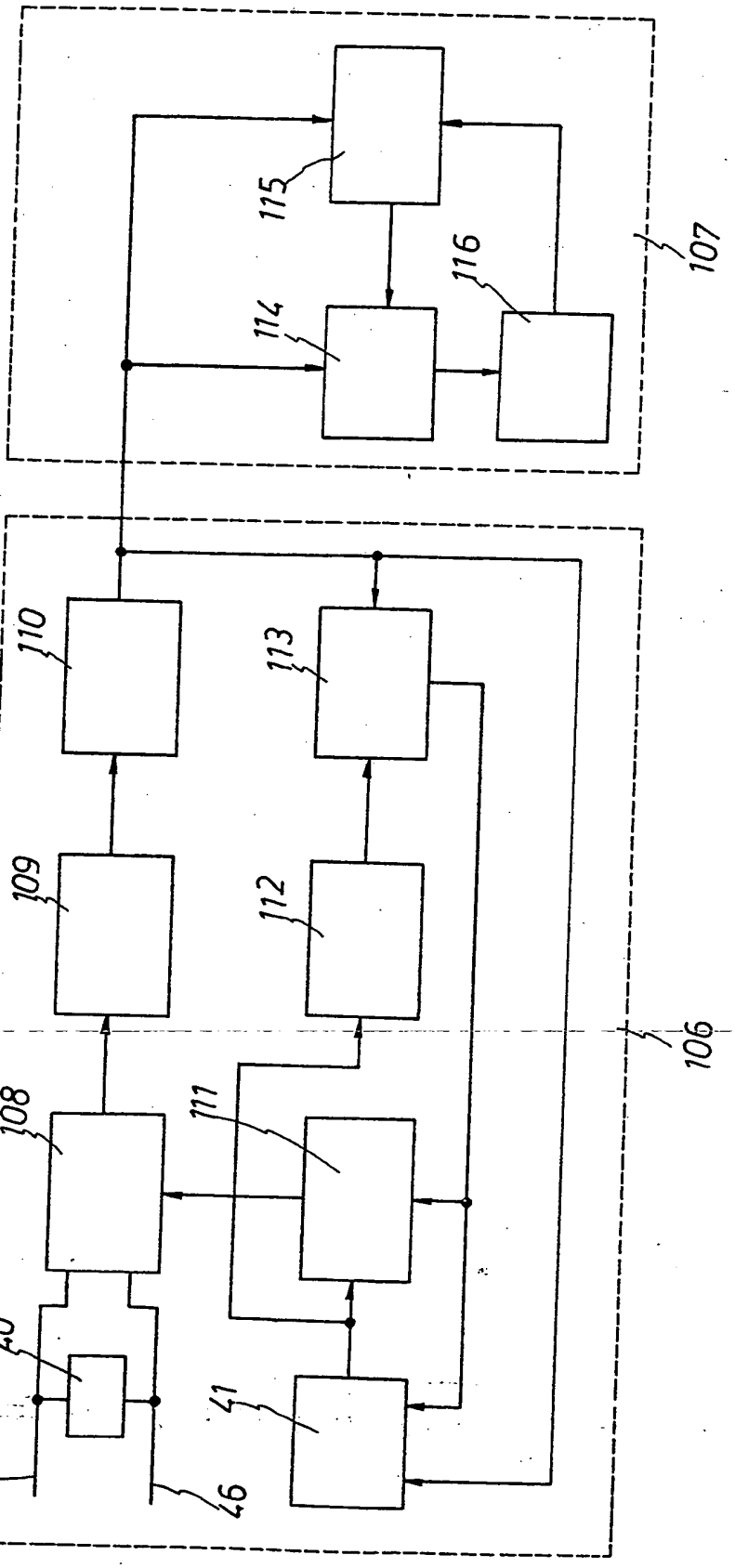
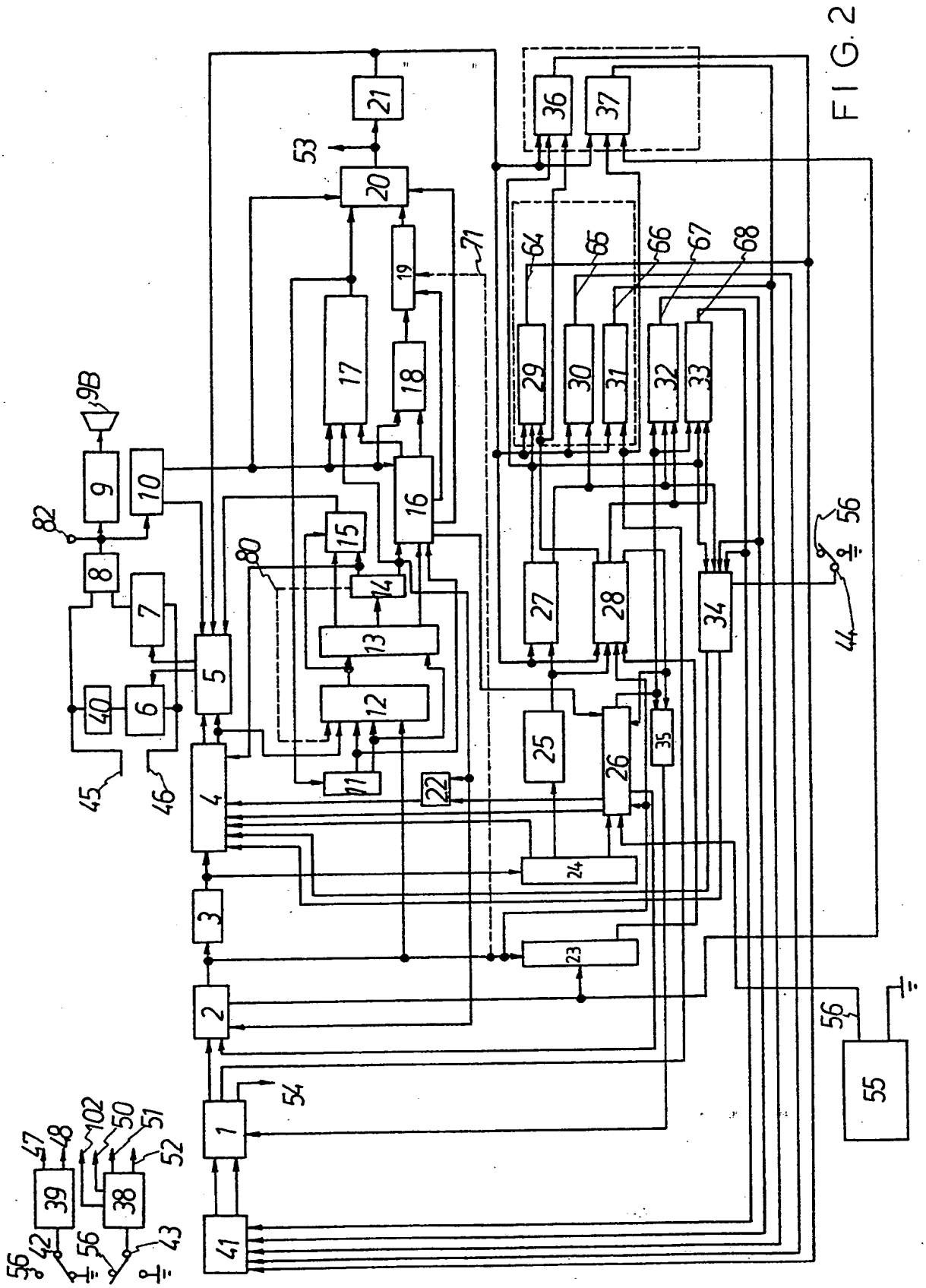


FIG. 1

FIG.2



2100890

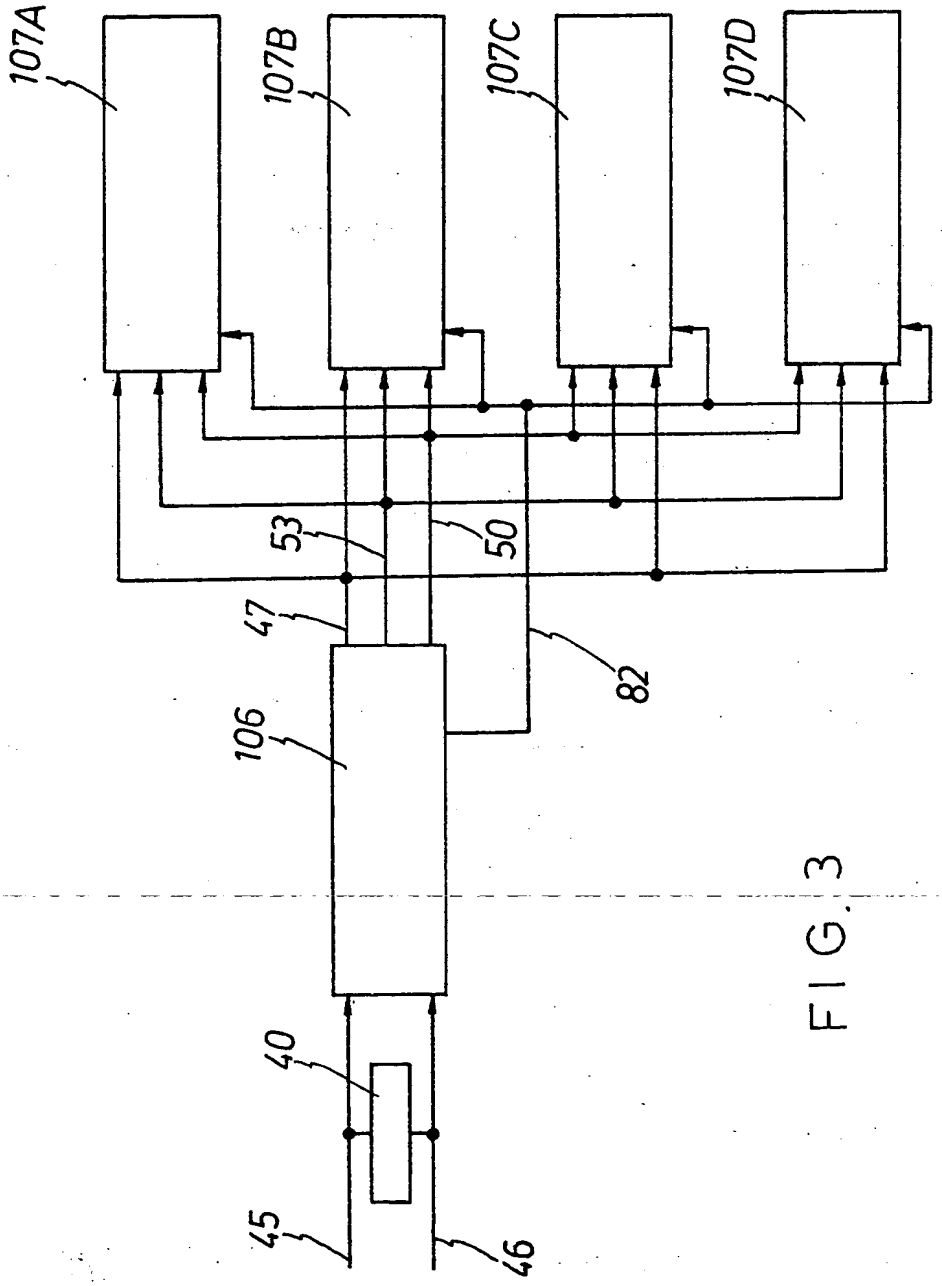


FIG. 3

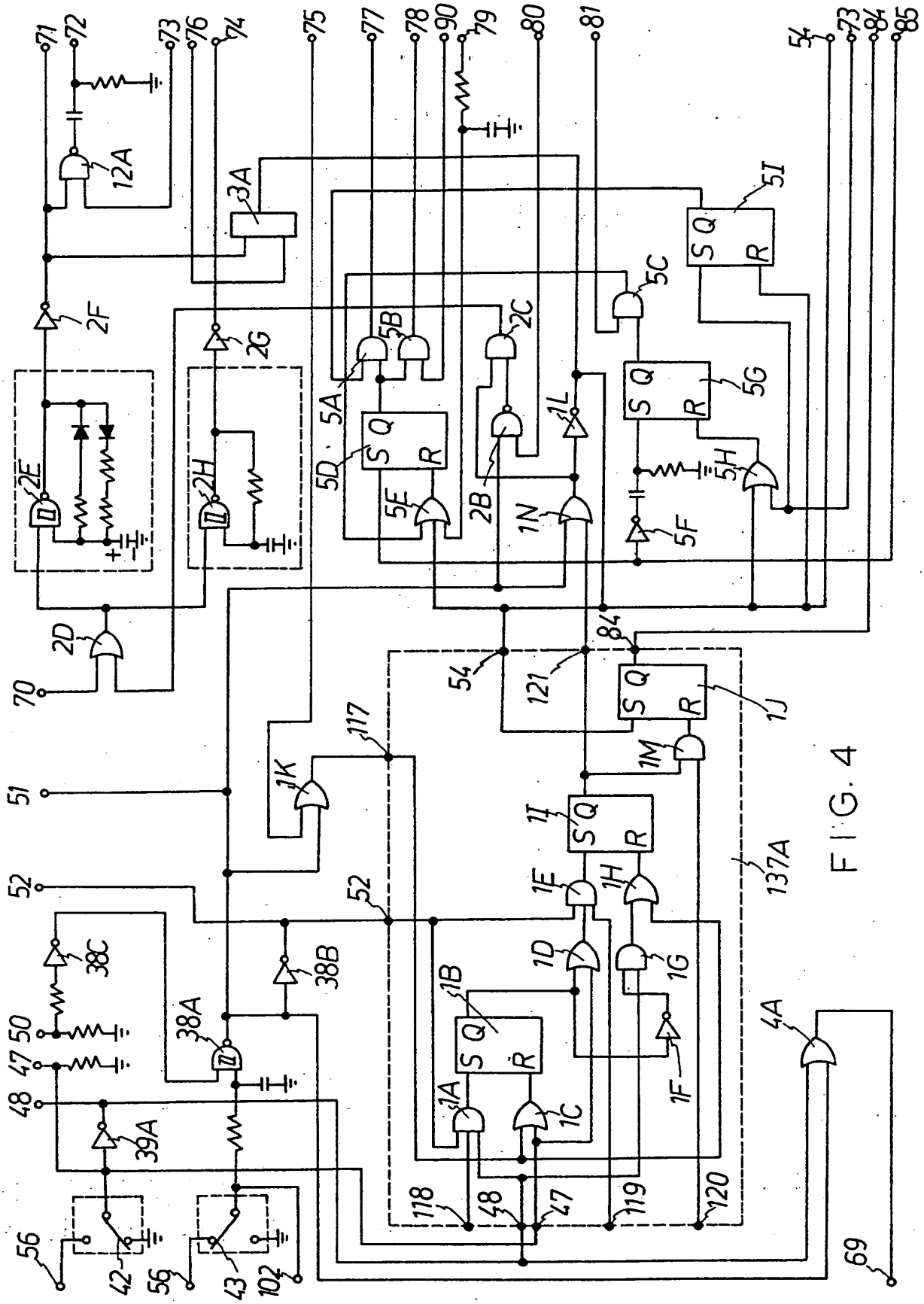


FIG. 4

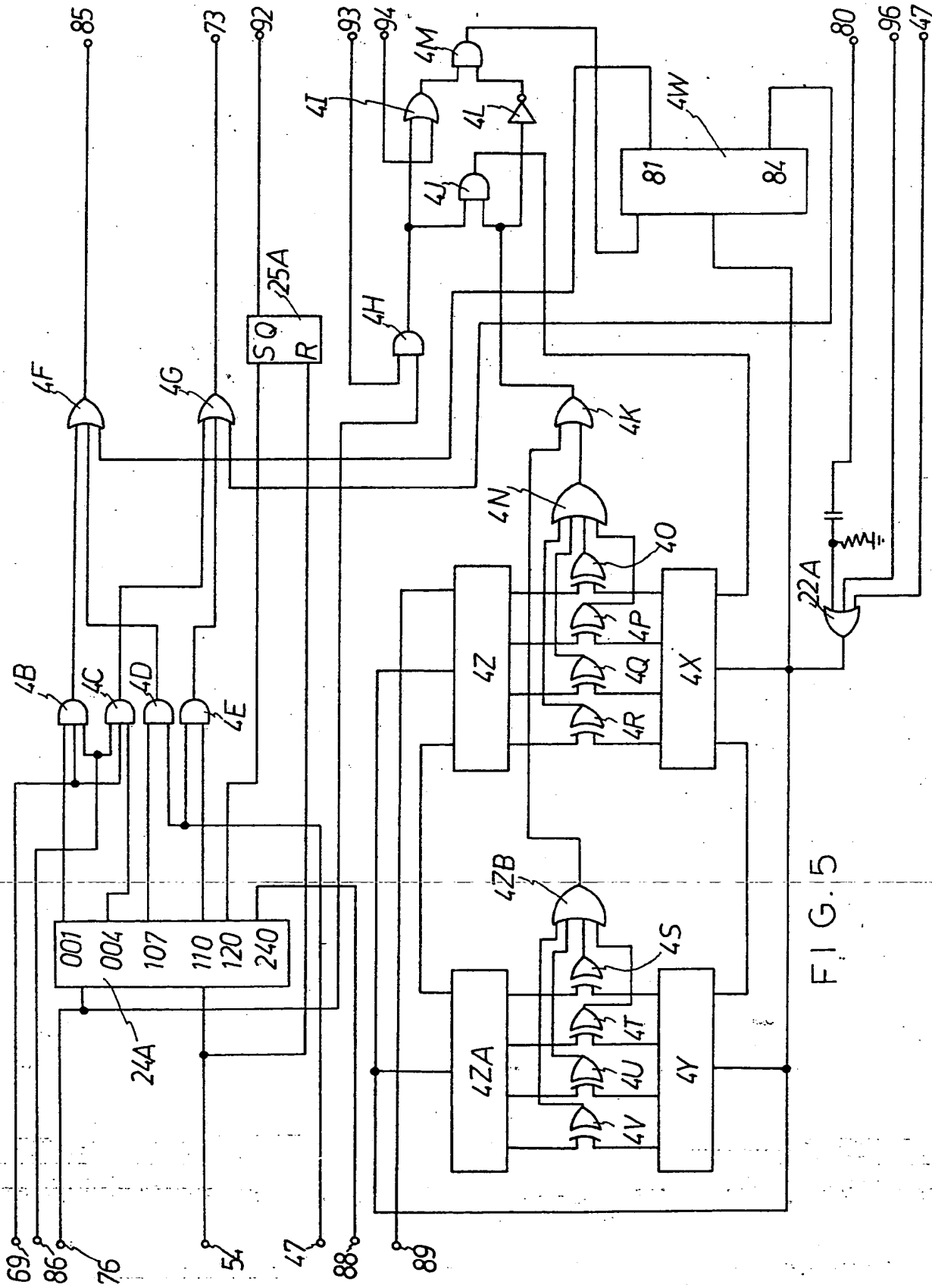


FIG. 5

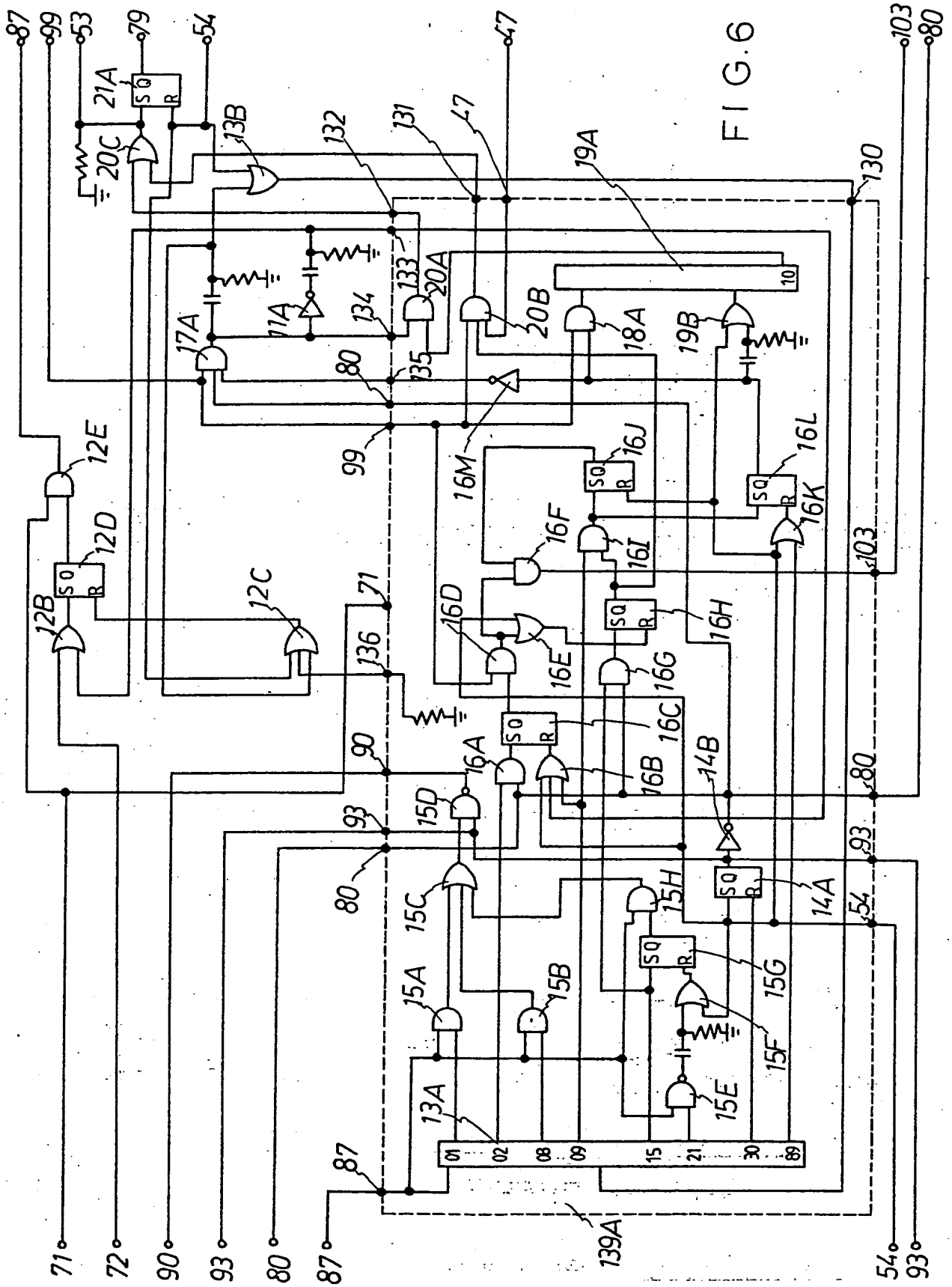


FIG.6

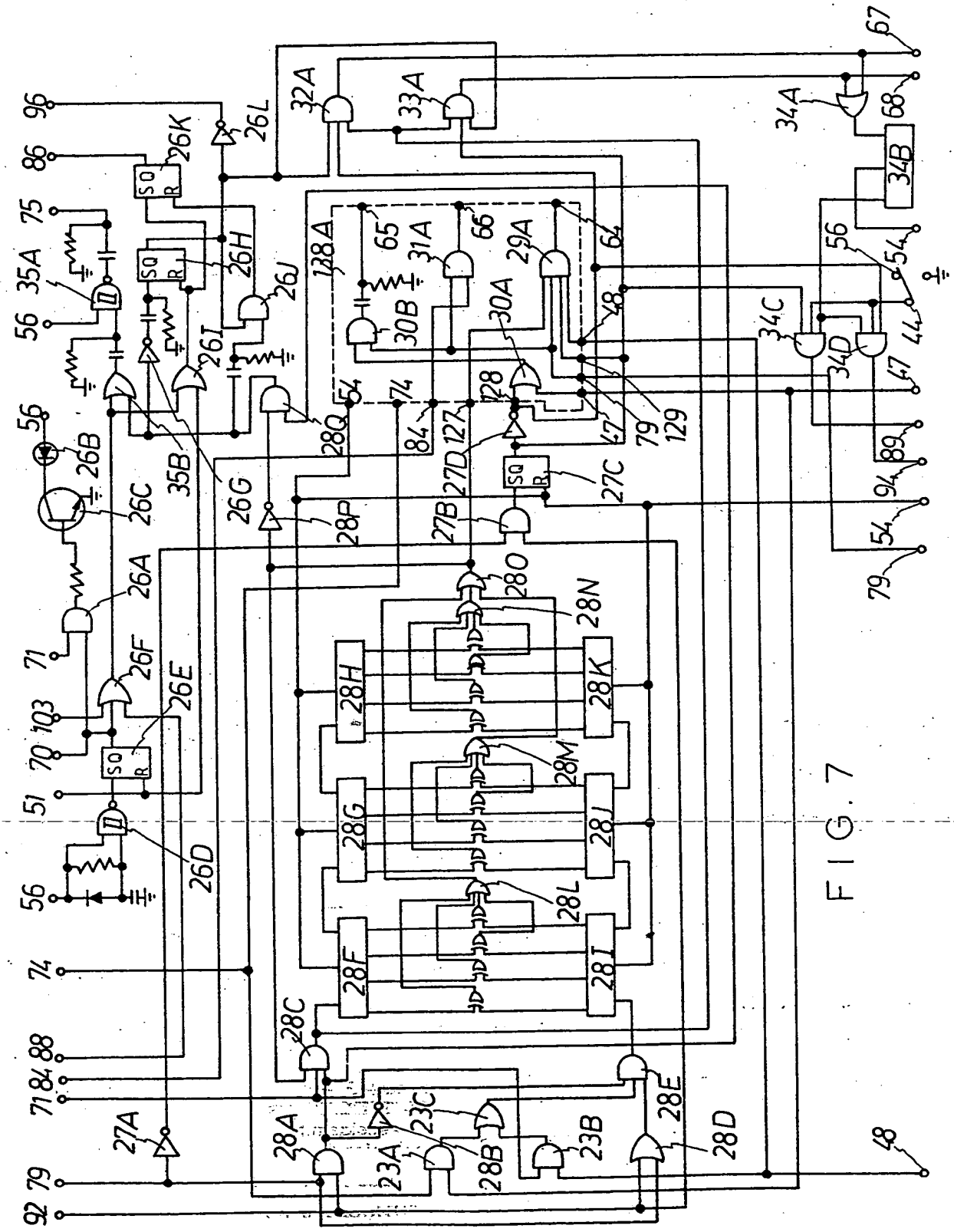


FIG. 7

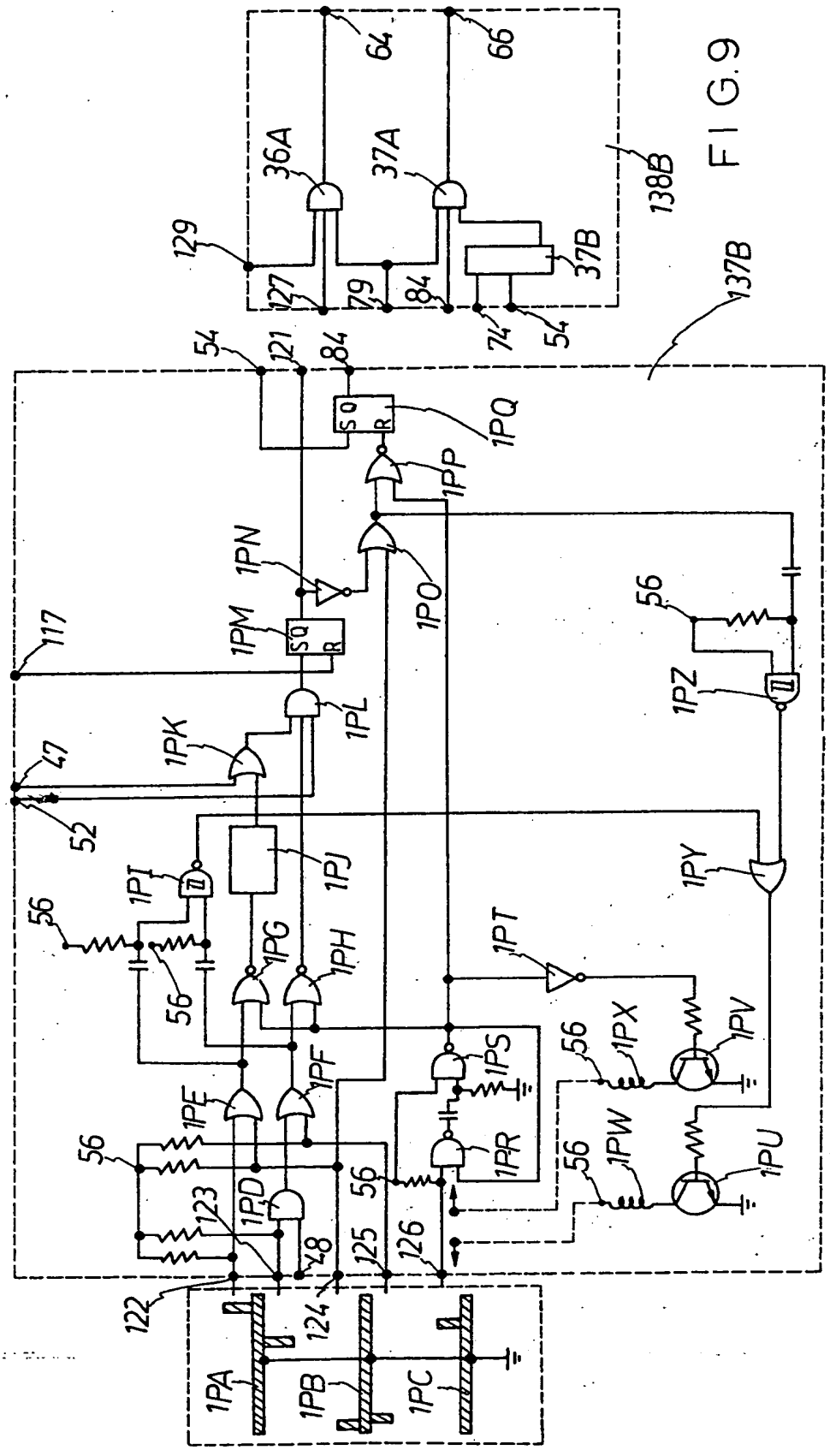


FIG. 9

FIG. 8

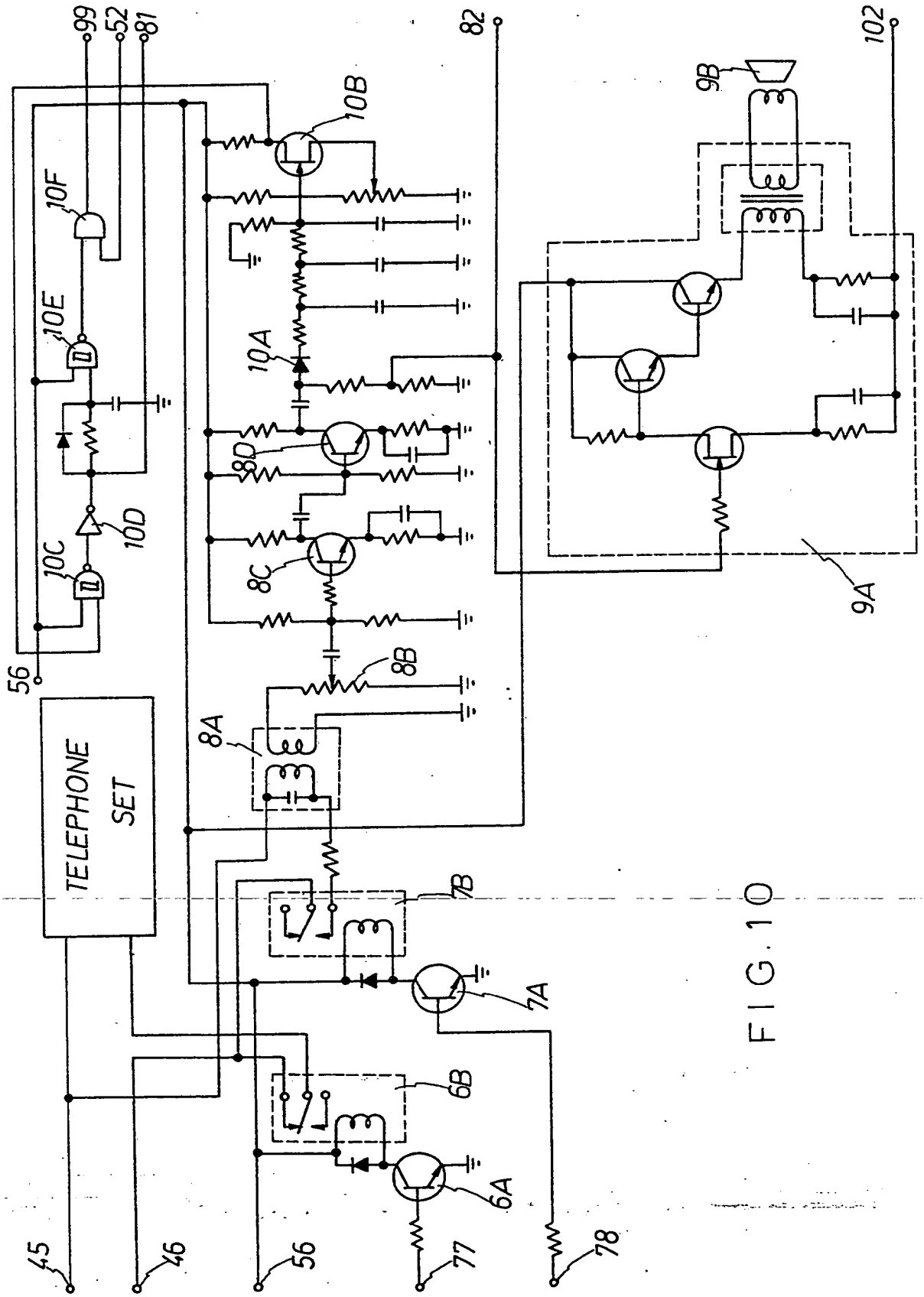


FIG. 10

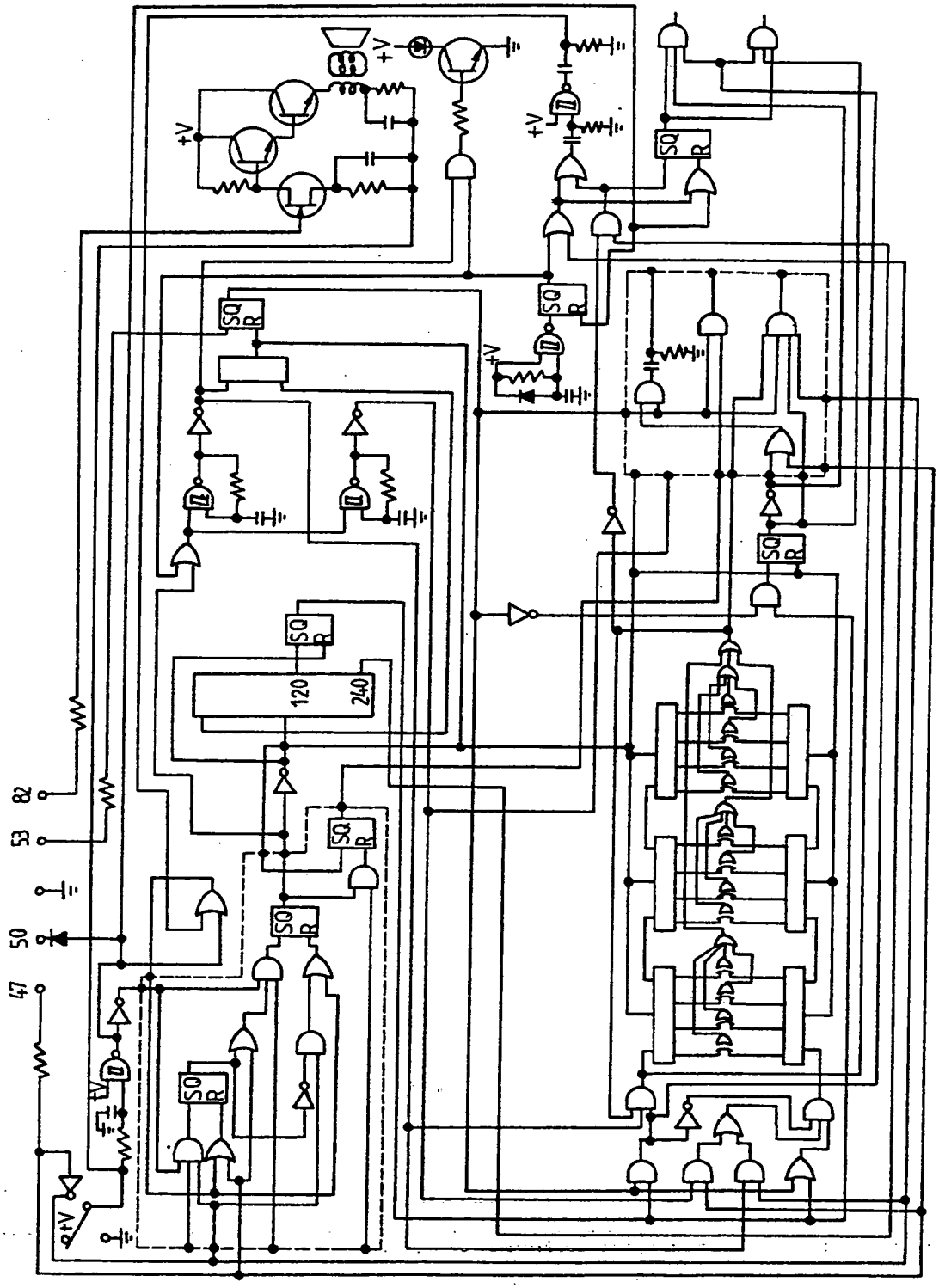


FIG.11

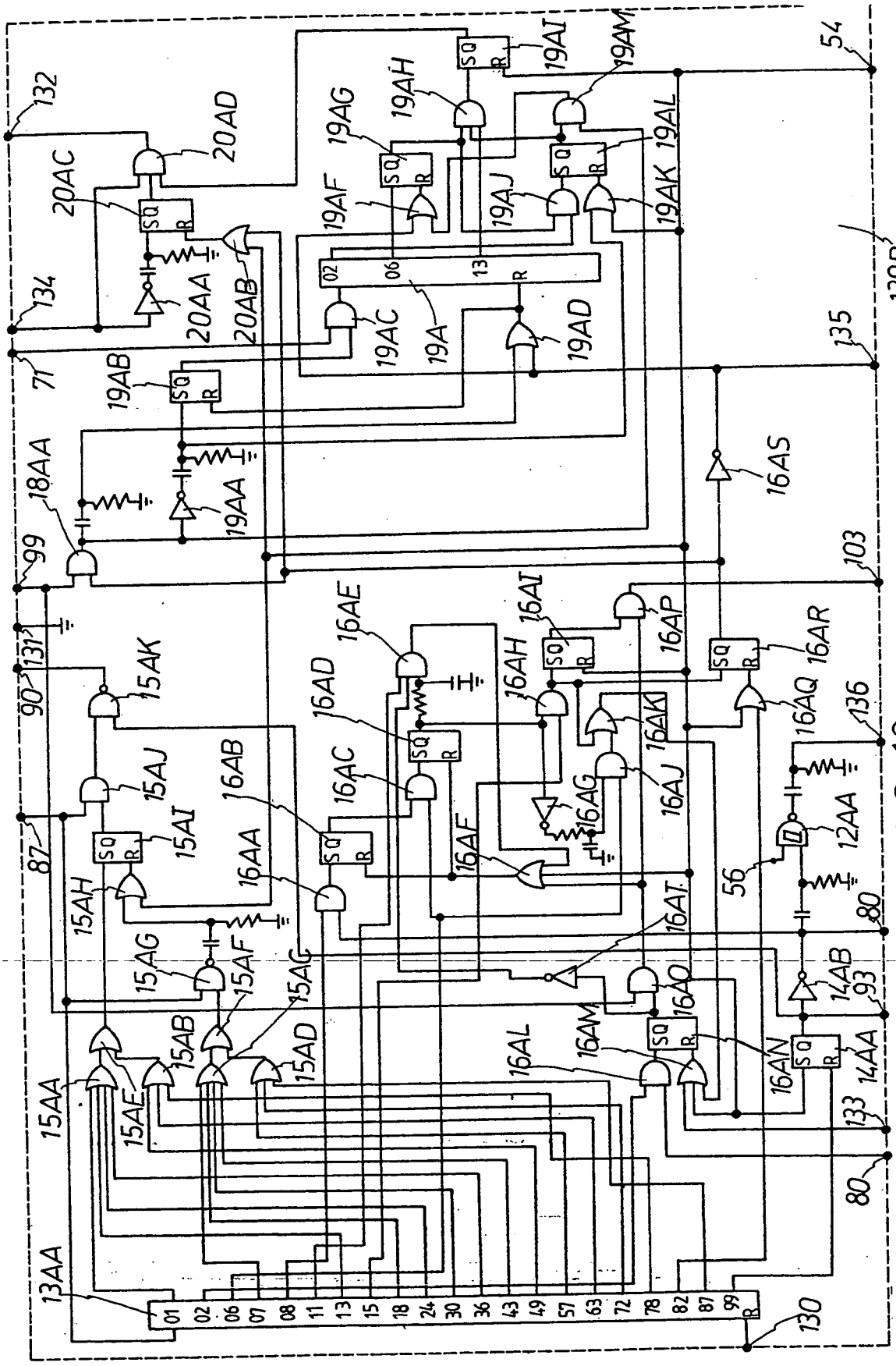


FIG. 12

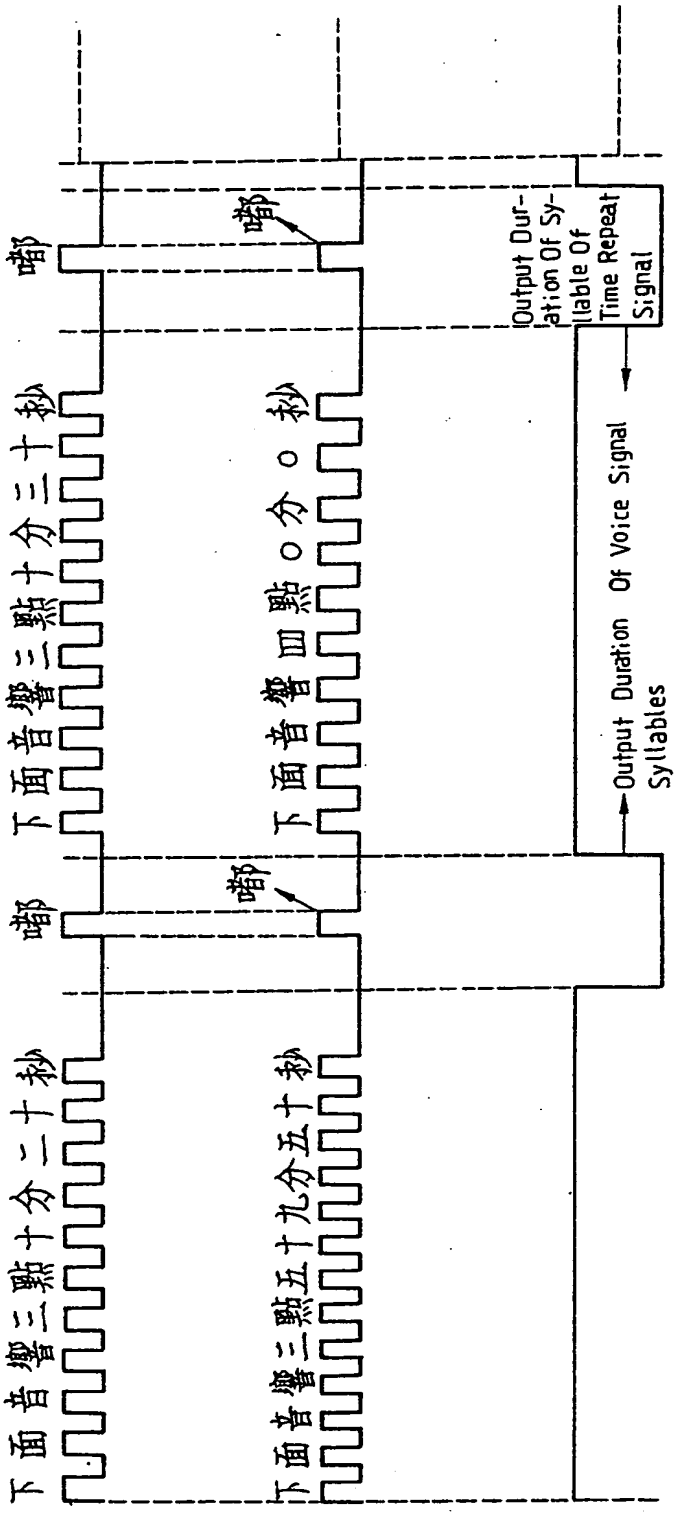


FIG.13

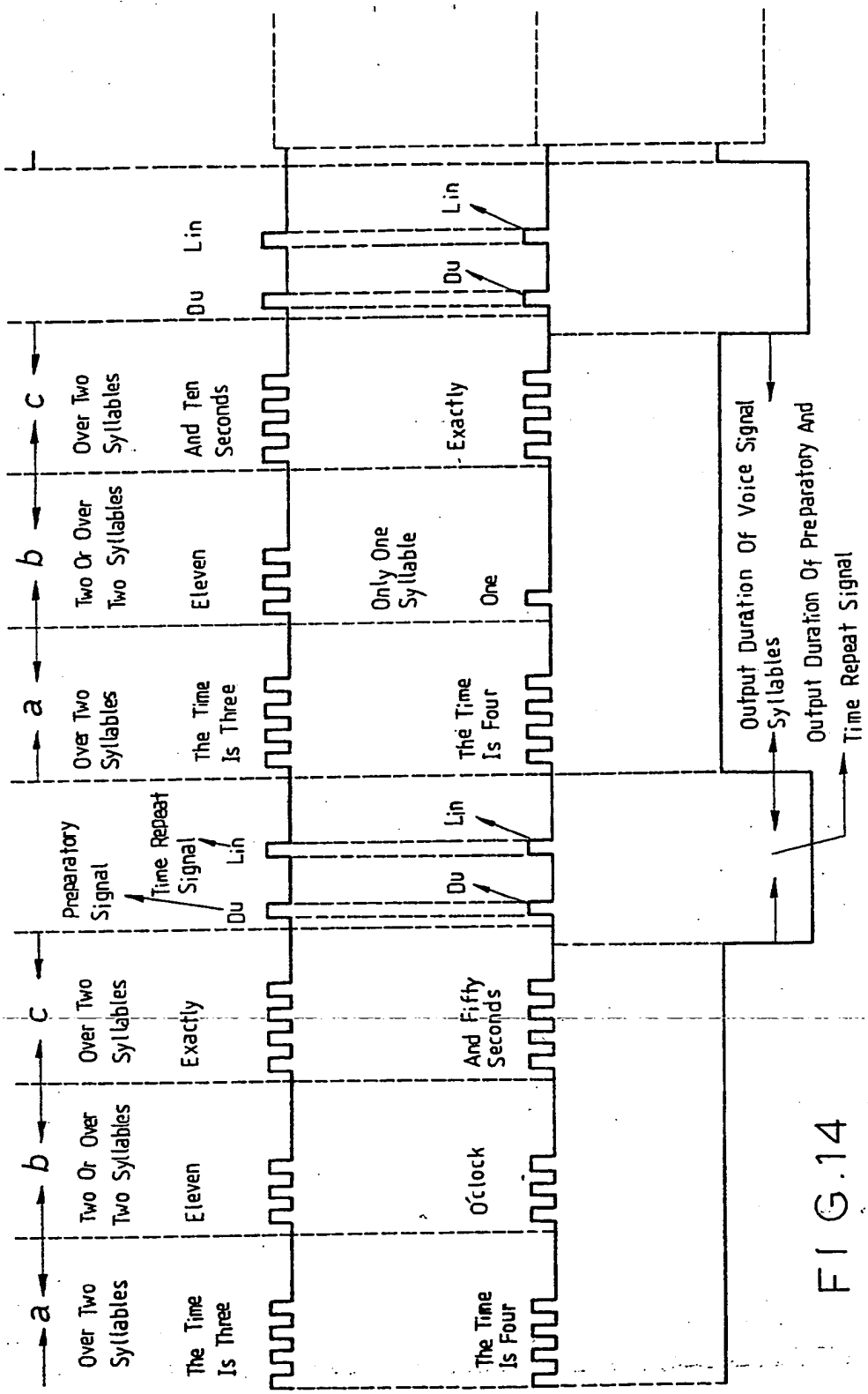


FIG.14

SPECIFICATION

A timepiece

The present invention relates to timepieces and is concerned with maintaining accurate time display by such timepieces.

The necessity and advantages of maintaining an accurate time display are well known, particularly where the timepiece is used by many people such as in a factory or a transport terminus.

According to a first aspect of the present invention there is provided a timepiece comprising means for periodically and automatically connecting the timepiece to a standard time signal *via* a telephone system and means for automatically synchronising the timepiece with the standard time signal.

According to a second aspect of the present invention there is provided a method of automatically maintaining the accuracy of the timepiece comprising periodic and automatic connection to a standard time signal *via* a telephone system and automatic synchronisation with the standard time signal.

This invention may provide a timepiece with an automatic time setting system *via* a dialled telephone line and an automatic speed adjusting system, which comprises a primary timepiece and a secondary timepiece. Prior to time calibration, the primary timepiece selects a suitable time to dial the telephone number of a standard time signal or time repeat station, and also identifies the information presented by the time repeat station. When the required standard time signal occurs, the primary timepiece and the secondary timepiece are automatically calibrated with the standard time. Simultaneously, the two timepieces can check their respective time differences and automatically adjust their speed or frequency. Thus, a timepiece system having an automatically maintained accuracy may be provided by this invention.

Embodiments of the present invention will now be described by way of example only, and with reference to the accompanying drawings, in which:

Figure 1 shows a system block diagram of an embodiment of the present invention;

Figure 2 shows a block diagram of the primary timepiece of the embodiment shown in Figure 1;

Figure 3 shows the system connection diagram between the primary timepiece and the secondary timepiece of the embodiment shown in Figure 1;

Figures 4, 5, 6 and 7 show detailed circuitry for respective portions of the primary timepiece illustrated in Figure 2;

Figure 8 shows interface circuitry suitable for use with an analog form of time display;

Figure 9 shows a time calibration control circuit of the present embodiment for use with an analog form of time display;

Figure 10 shows the control and the monitor circuit of the present embodiment connected to a telephone system;

Figure 11 shows a circuit diagram of the secondary timepiece;

Figure 12 shows an automatic dial and time signal separation control circuit suitable for use with the American type of standard time signal available on the general telephone system;

Figure 13 is a diagram of the Chinese type of telephone standard time signal system including the respective signal syllables; and

Figure 14 is a diagram of the American type of telephone standard time signal system including the respective signal syllables.

The illustrated embodiment, which is described in detail below, seeks to provide the following features:

(A) prior to calibration of the timepiece, the timepiece automatically connects itself to the telephone standard time signal by dialling the relevant telephone number;

(B) automatic synchronisation with the telephone standard time signal;

(C) automatic adjustment of the frequency or running speed of the timepiece in accordance with the magnitude of the adjustment required to obtain synchronisation, such that accumulative time differences compared with the standard time are minimised;

(D) automatic synchronisation and automatic adjustment of frequency within a time tolerance of plus or minus twenty minutes;

(E) automatic adjustment of the time of dialling the standard time telephone number in accordance with variation from the standard time, in order to minimise the length of time for which the telephone line is used;

(F) operator determination of the period between successive synchronisation and speed adjustments, for example once a day, once an hour, or other desired period;

(G) by means of a time signal and vocal signal separation circuit, the time signal and the vocal signal are identified by the silent intervals between adjacent signals and by means of a vocal signal discrimination circuit, the time calibration signals are identified by the number of syllables in the vocal signal. The standard time signal or time calibration signal initiates the automatic synchronisation or calibration and the speed adjustment operations;

(H) because of the ability of the primary timepiece to automatically connect and synchronise with a standard time signal, several secondary timepieces, of simple structure, may be connected to the primary timepiece and hence a single telephone line may be utilised to automatically synchronise and automatically adjust the running speed of a plurality of timepieces;

(I) the timepieces may be provided with either analog or digital time displays;

(J) the timepieces may be powered by an AC power supply, a DC battery, or by means of a mechanical spring.

Figures 1 and 2 show block diagrams and the primary timepiece. The circuits can be used

together with a digit timepiece or a hand timepiece, or a mechanical spring timepiece 41. A system block diagram of an embodiment is shown in figure 1, which comprises the primary timepiece 106 and the secondary timepiece 107; further, the said primary timepiece 106 comprises the automatic dial circuit 108, the separating circuit of time repeat signal and voice signal 109, the identifying circuit of voice signal and the analyzing circuit of time calibration signal 110, the conventional timepiece 41, the telephone line switching circuit and the automatic adjusting circuit of dialing starting time 111, the synchronous time counting circuit of timepiece 112, the synthetic circuit of time differential signal 113. The said secondary timepiece 107 comprises the conventional timepiece 114, the synthetic circuit of time differential signal 115, and the synchronous time counting circuit of timepiece 116.

Figure 3 is a block diagram of the whole system of embodiment No. 1 of this invention, in which the primary timepiece 106 block diagram comprises, as shown in figure 2, the conventional timepiece 41, the interface circuit 1, the oscillation circuit 2, the divider 3, the telephone line switching circuit and automatic adjusting circuit of dialing starting time 4, the telephone line monitor circuit 5, the telephone set separation circuit 6, the telephone line switching and dialing circuit 7, the audio frequency amplifier 8, the audio frequency separation and amplification circuit 9, speaker 9B, the syllable generating circuit 10, the differential circuit 11, the switch of dialing pulse and syllable interval timing circuit 12, the dialing pulse and syllable interval timing circuit 12, the switching circuit 14, the generating circuit of dialing pulse 15, the separating circuit of telephone time signal and voice signal 16, output circuit of time signal 17, output circuit of voice signal 18, discrimination circuit of voice signal 19, the analyzing circuit of time signal designed for time calibration 20, the signal resetting circuit 22, the output circuit of time signal designed for time calibration 21, the frequency selection switch circuit 23, the synchronization timing circuit 24, the output circuit of time signal designed for time calibration 25, the system trouble monitor circuit 26, the time difference advance/lag discrimination circuit 27, the count circuit of time difference 28, the circuit of stopping (holding) signal output 29, the "zero" second setting (seconds and 10's of seconds reset to zero) differential signal output circuit 30, fast set control signal output circuit 31, the speed increasing control signal output circuit 32, the speed reducing control signal output circuit 33, the divider 34, time delay circuit 35, the circuit of stopping signal output 36, the second hand fast rotating signal output circuit 37, the time repeat monitor circuit 38, the selection circuit of time calibration frequency 39, the telephone 40, the power supply circuit 55, and switches 42, 43 and 44.

The circuit and theory of the primary timepiece as shown in embodiment No. 1 are explained as follows:

1. Analysis of the characteristics of telephone time repeat system:

(1) Figure 13 shows the Chinese type of telephone time repeat system and the syllable of time repeat signal; thru the syllable of figure 13, some characteristics may be analyzed as follows:

(A) Between the syllable of time repeat signal (Du . . .) and the adjacent syllables, there is a longer silent interval, while there is no such condition existing in other voice syllables. In the circuit of primary timepiece as shown in embodiment No. 1, the said characteristic is used for separating the time repeat signal and the voice signal.

(B) From 10 minutes and 20 seconds passes every hour thru 10:59 and 50 seconds), the number of voice syllables of every 10 seconds generated is more than that of being generated during the time of zero minute and zero second of next hour (For example, during the period from 3:10 and 20 seconds thru 3:59 and 50 seconds, the voice syllables generated in 10 seconds are more than ten each, but at 4:00 sharp, the voice syllables generated will reduced to ten suddenly.

Therefore, when this invention is used for the Chinese type of time repeat system, the time selected for time calibration is at zero minute and second of every hour (It is better to select a moment in the early morning, during which the telephone line is not busy and almost everyone is in deep sleep). By the same token, the time repeat signal at "zero minute and zero second" is picked up from the circuit of the primary timepiece as shown in embodiment No. 1 in accordance with the number of voice syllables, and will be used as a reference signal. The system mentioned in 1 above is good for use in the country of which the syllable is clear or one word having one syllable, such as China, Japan, and Korea, etc. The embodiment No. 1 is good for the Chinese type of time repeat system, and its explanation is based on a design set at 04:00 AM.

(2) Figure 14 shows the American type of telephone time repeat system and the syllable of time repeat signal; thru the syllable of figure 14, some characteristics may be analyzed as follows:

(A) Between the preparatory signal (Du . . .) the time repeat signal (Lin . . .) and the adjacent syllable, there is a longer silent interval, while there is no such condition existing in other voice signal syllables. In the circuit of primary timepiece as shown in embodiment No. 1, the said characteristic is used for separating the time repeat signal (including the preparatory signal) and the voice signal.

(B) The voice signal appears in a, b, c, syllable groups, and between the said syllable groups, there is a longer silent interval; in the syllable groups "a" and "c", there are at least two or more syllables, while in the syllable group "b", there is one, or two, or more than two syllables.

From 11 minutes and zero seconds passed every hour thru zero minute and 50 seconds of

next hour, there are two or more than two voice syllables appearing in syllable group "b" every 10 seconds; then, at one minute and zero second, the number of voice syllable is suddenly reduced to one syllable (during this time, there is only one syllable in between the two long silent intervals.

When this invention is used for American type of time repeat system, the calibration time is designed to set at one minute and zero second of any hour (However, it is better to select a moment in the early morning, during which the telephone line is not busy and almost everyone is in deep sleep). Consequently, the time repeat signal at "one minute and zero second" is picked up (to bypass the preparatory signal first) in accordance with the number of syllables appeared in the aforesaid syllable group "b" as shown in the circuit of primary timepiece in embodiment No. 1, and will be used as a reference signal.

The said system mentioned in 2 above is good for the time repeat system in all Teuton or Latin language countries, such as the States, and European countries etc. The embodiment No. 1 is good for the American type of time repeat system, and its explanation is based on a design set at 04:01 and zero second AM (It may be set at any suitable time).

2. When the circuit of primary timepiece in embodiment No. 1 is in the normal stable state, the outputs of "Q" terminal of the NOR R/S LATCH 5 are all LOW except the 1J, 14A, 26H, 1PQ, 14AA which are all HIGH. (Figures 4, 6, 7, 8, 12).

3. The conventional timepiece 41 will at 03:00 AM, have an output of HIGH pulse, which will, thru the lead-in wire 118 and the AND GATE 1A, change the LOW output of the Q terminal of NOR R/S LATCH 1B (Fig. 4) into HIGH. When the said conventional timepiece 41 is at 03:38 (It may be set at a time other than the aforesaid time; if the time is set at 03:35, the maximum time tolerance difference will be about $\pm$25 minutes), it will generated another output of HIGH pulse, which will, thru lead-in wire 119 and the AND GATE 1E, change the LOW of Q terminal or NOR R/S LATCH 1I into HIGH; then, thru the lead-in wire 121, the OR Gate 1N, the AND GATE 2C, and OR GATE 2D, the pulse will have the OSC comprising SCHMITT TRIGGER 2E and 2H starting to oscillate, and the said two trigger circuits will generate their outputs thru the INVERTER 2F and 2G respectively. The circuit of SCHMITT TRIGGER 2E is a non-equilibrium square wave OSC. of 10 HZ, and its each cycle of HIGH output takes 67 ms, while its each cycle of LOW output takes 33 ms.; on the contrary, the circuit of SCHMITT TRIGGER 2H is an equilibrium square wave OSC. of 240 HZ (for more details, see figure 4).

If the timepiece is a hand type (analogue display), the dotted line portion 137A in figure 4 and 138A in figure 7 should be replaced with the dotted line portion 137B of figure 8 and the portion 138B of figure 9, and the rest circuits remain unchanged. Figure 8 is the interface circuit being used together with the general hand type timepiece in embodiment No. 1 of this invention, in which 1PA is the hour wheel, and 1PB is the minute wheel, and on each side of the upper and lower edge of said wheel, a pin is installed; 1PC is the second wheel, of which on the upper edge, a pin is installed; When the said upper three pins of three wheels are superimposed on one straight line, the time would be 00:00 hour, or 12:00. When the pins under the hour wheel and the minute wheel, and the pin on the second wheel are superimposed on one straight line, the time would be 03:58 and zero second (It may be set at different time). The diameter of pins on the hour wheel and the minute wheel is bigger than that of pin on the second wheel; the said three wheels are all earthed. The lead-in wires (122, 123, 124, and 125) are all made of fine steel wire having elasticity, and are all attached on a fixed position. When the hour wheel and the minute wheel rotate to the straight line between the lead-in wire and the wheel axle, the lead-in wire will touch the pin. The lead-in wire 126 made of fine steel wire with elasticity can be moved forwards and backwards: when the circuit is in stable state, the said lead-in wire is at its rear position and will not touch the pin of second wheel. When the pin of the second wheel rotating to the straight line between the lead-in wire and the wheel axle, when the said lead-in wire is moved to its front position, the lead-in wire will touch the said pin immediately.

When the upper pins of the hour wheel, the minute wheel and the second wheel are almost superimposed on a straight line, the pins of the hour wheel and minute wheel will first touch the lead-in wires 122, 124 because of the diameter of said pins is bigger than that of pin of the second wheel; then the OR GATE 1PE will have an output of LOW, which will, thru the differential circuit and SCHMITT TRIGGER 1PI, have a pulse output, and the said pulse will go thru OR GATE 1PY, TRANSISTOR 1PU, and the relay 1PW to cause the lead-in wire 126 going forwards; when the said three pins are superimposed on a straight line, the pin of second wheel will touch the lead-in wire 126. If the aforesaid touching moment is at 00:00 hour the HAND GATE 1PS will have an output of negative pulse, which will, thru NOR GATE 1PG, cause the T FLIP/FLOP 1PJ having an output of HIGH so as to change PM into AM; at the same time, the said negative pulse will go thru INVERTER 1PT, TRANSISTOR 1PV and relay 1PX to cause the lead-in wire 126 going backwards. When the said lead-in wire touching the pin of second wheel, it goes backwards immediately, in other words, the touching time is very short. By the same token, when the pin under the bottom side of the hour wheel and the minute wheel and the pin of second wheel are superimposed on a straight line, the lead-in wires 123, 125 will first touch pins, and the OR GATE 1PF will have an output of LOW, which will, thru the differential circuit, cause the SCHMITT TRIGGER 1PI to have a pulse output so as to drive the lead-in wire 126 going forwards. When the three pins are

superimposed on a straight line, the pin of second wheel touches the lead-in wire 126 and the time is 03:58 AM (It may be set at different time); then the NAND GATE 1PS will have an output of negative pulse, which will go thru NOR GATE 1PH and the AND GATE 1PL to cause the "Q" terminal of NOR R/S LATCH 1PM changing to HIGH going to the following stage thru lead-in wire 121; at the same time, the said negative pulse will go thru the INVERTER 1PT to cause the lead-in wire 126 going backwards. By the same token, when the upper two pins of the minute wheel and the second wheel are almost superimposed on a straight line, the lead-in wire 124 will first touch the pin, and the OR GATE 1PO will have a LOW output, which will, thru the differential circuit, cause the SCHMITT TRIGGER 1PZ having a pulse output to move the leading wire 126 forwards; when the two pins being superimposed on a straight line, the pin of the second wheel will touch the lead-in wire 126; now, we use the said moment as the time of calibration, i.e., 04:00 AM (For the American type, it is 04:01 and zero second); then, the NAND GATE 1PS will have an output of negative pulse, which will, thru NOR GATE 1PP, cause the "Q" terminal of NOR R/S LATCH 1PQ changing into LOW which will become an output thru lead in wire 84 (For the circuit to be continued, see the explanations in item 11); at the same time, the said negative pulse will, thru INVERTER 1PT, cause the lead-in wire 126 going backwards.

4. As shown in figure 4 and 5, INVERTER 2F will transmit a pulse 10 HZ to DIVIDER 3A where the said 10 HZ pulse is divided by 10; then, a pulse of 1HZ is, thru lead-in wire 76, delivered to COUNTER 24A so as to start counting the time together with the timepiece 41 on a synchronization basis; simultaneously, the said pulse of 1 HZ is delivered to the input terminal of AND GATE 4H.

5. COUNTERS 4Z and 4ZA are the "ahead of time difference memory circuit of timepiece 41", and COUNTER 4W is the "behind time difference memory circuit of timepiece 41", if the timepiece 41 is faster than the standard time the COUNTERS 4Z and 4ZA will record and store a time difference signal, comparing with COUNTERS 4X and 4Y; then a non-equilibrium state will exist; consequently, the OR GATE 4K will have an output of HIGH, and the aforesaid pulse of 1HZ will, thru AND GATE 4H and 4J, go into COUNTERS 4X and 4Y for counting numbers As soon as the counting is equal to the time difference stored in COUNTERS 4Z and 4ZA, the output of OR GATE 4K will turn to LOW, and the output of INVERTER 4L will also turn to HIGH; simultaneously, the pulse of 1 HZ will, thru OR GATE 4I and AND GATE 4M, be delivered to COUNTER 4W for continuously counting. If the timepiece 41 is behind the standard time, the aforesaid pulse of 1 HZ will, thru AND GATE 4H, OR GATE 41, and AND GATE 4M, be delivered to COUNTER 4W for accumulating counting. When the COUNTER 4W is counting to number 81 which is approximately at 03: 59 and 21 seconds of standard time (It may be set at a different moment), the said counter 4W will have an output of HIGH, which will go thru OR GATE 4F and the lead-in wire 85 to have the "Q" terminal of NOR R/S LATCH 5D generating an output of HIGH; then, the said HIGH signal will go thru AND GATE 5B, lead-in wire 78, TRANSISTOR 7A, and RELAY 7B to have the telephone line 46 being connected with the COUPLING TRANSFORMER 8A as shown in figure 4, 5, and 10. At the same time, the HIGH pulse output of COUNTER 4W will go thru INVERTER 5F to have the "Q" terminal of NOR R/S LATCH 5G appearing an output of HIGH within one second; after two seconds from that moment, the voice signal, if the telephone set being used, will go thru lead-in wire 81 AND GATE 5C, and OR GATE 5E to have the HIGH at "Q" terminal of NOR R/S LATCH 5D changing into LOW, and the said LOW will cause the COUPLING TRANSFORMER 8A being separated with telephone line 46. On the other hand, if the telephone set is not used and the COUPLING TRANSFORMER 8A is connected with the telephone line 46, and the telephone set has a continuous "hum" signal, the lead-in wire 81 will be in LOW state, and the "Q" terminal of NOR R/S LATCH 5D will remain in HIGH state, and the COUPLING TRANSFORMER 8A remains being connected with the telephone line 46 as shown in figures 4, 5, 10. When the COUNTER 4W continuously counts to 84, which is approximately equal at the standard time of 03:59 and 24 seconds (It may be set at a different moment), it will have an output of HIGH pulse, which will go thru OR GATE 4G, lead-in wire 73, and OR GATE 5H to have the "Q" terminal of NOR R/S LATCH 5G changing to LOW, and simultaneously to have the "Q" terminal of NOR R/S LATCH 5I changing to HIGH; then, the said HIGH will go thru AND GATE 5A, lead-in wire 77, TRANSISTOR 6A, and RELAY 6B to have the telephone line 46 being separated with telephone set 40 as shown in figures 4, 5, 10.

As shown in figure 10, the signal from the telephone lines 45, 46 will go thru the two stage amplifier comprising COUPLING TRANSFORMER 8A and TRANSISTORS 8C and 8D, the diode 10A rectifier, the RC filter, and the FET 10B amplifier, and finally is delivered to SCHMITT TRIGGER 10C and 10E to generate syllable square wave, which will further go thru AND GATE 10F and lead-in wire 99 being coupled to next stages.

6. The pulse output of the aforesaid COUNTER 4W when counting to 84 will go thru lead-in wire 73 to enter into the NAND GATE 12A together with the non-equilibrium square wave of 10 HZ from INVERTER 2F; then, thru the differential circuit, the lead-in wire 72 and OR GATE 12B to have the "Q" terminal of NOR R/S LATCH 12D appearing an output of HIGH; at the same time, the non-equilibrium square wave of 10 HZ (HIGH 67 ms, LOW 33 ms) will go thru AND GATE 12E and the lead-in wire 87 to enter into COUNTER 13A for counting. When the first pulse of 10 HZ

entering into COUNTER 13A, said COUNTER 13A will also deliver an output pulse to enter into AND GATE 15A will also deliver an output pulse to enter into AND GATE 15A simultaneously with the first pulse of 10 HZ; then the AND GATE 15A will generate a dial pulse of 67ms, and when the 8th pulse entering into AND GATE 15B, it will also generate a dial pulse of 67 ms; when the 15th pulse entering into the input, NOR R/S LATCH 15G will have a HIGH at its "Q" terminal so as to have the 10 HZ pulse, thru AND GATE 15H, continuously going forwards as an output until the 21st pulse entering and thru NAND GATE 15E, the differential circuit, and the OR GATE 15G to cause the "Q" terminal of NOR R/S LATCH 15G changing into LOW. During the period of the "Q" terminal of NOR R/S LATCH 15G being in HIGH state, there is a total of 7 dial pulses being delivered continuously from AND GATE 15H; the aforesaid dial pulses means the telephone number of the time repeat station and all the said pulses will go thru OR GATE 15C, NAND GATE 15D, the lead-in wire 90, AND GATE 5B, lead-in wire 78, and TRANSISTOR 7A to cause the relay 7B generating a dialing action (more details, see figures 4, 5, 6, 10).

When the 30th pulse of 10HZ entering into COUNTER 13A, it will generate a pulse to cause the "Q" terminal of NOR R/S LATCH 14A changing to LOW, and to cause the output signal of OR GATE 15C not going thru NAND GATE 15D, and at the same time, thru lead-in wire 93 entering into AND GATE 4H to stop the 1 HZ signal passing COUNTER 4W for counting; instead, the said signal will go thru INVERTER 14B, lead-in wire 80, the differential circuit and OR GATE 22A to have the COUNTER 4W, 4X, 4Y, 4Z and 4ZA being reset; for more details, see figures 5 and 6. When being used in American type of time repeat system, just change the dotted line portion 139A of figure 6 into the dotted line portion 139B of figure 12, and the rest circuits remain unchanged.

The number of time repeat station in the States is a 7-digit number; for instance, in California, the number is "7678900"; as shown in figures 4, 6, 10, 12 the non-equilibrium square wave of 10 HZ is, thru lead-in wire 87, entering into the COUNTER 12AA to start counting; when the first pulse entering into COUNTER 13AA, it will deliver a pulse going thru OR GATE 15AA and 15AE to cause the "Q" terminal of NOR R/S LATCH 15 AI changing to HIGH, and to cause the pulse of 10 HZ going thru lead-in wire 87, AND GATE 15AJ, NAND GATE 15 AK, lead-in wire 90, AND GATE 5B, lead-in wire 78, and TRANSISTOR 7A continuously so as to have the relay 7B generating a dialing action until the 7th pulse entering into COUNTER 13AA; the said COUNTER 13AA will deliver a pulse going thru OR GATE 15AC and 15AF and simultaneously and together with 10 HZ pulse entering into NAND GATE 15AG, the differential circuit, and OR GATE 15AH to cause the "Q" terminal of NOR R/S LATCH 15AI changing to LOW. During the period of the "Q" terminal of NOR R/S LATCH 15AI being in HIGH state, the AND GATE 17AJ have continuously generated 7 dialing pulses that stand for "7"digits; by the same token, the 13rd thru 18th pulse stand for "6"; the 24th thru 30th pulse stand for "7", the 36th thru 43rd pulse stand for "8"; the 49th thru 57th pulse stand for "9"; the 63rd thru 72nd pulse stand for "0"; the 78th thru 87th pulse stand for "0" the pulses generated by AND GATE 17AJ are the dialing pulses for the number of time repeat station. When the 99th pulse of 10HZ entering into COUNTER 13AA, it will generate a pulse to cause the "Q" terminal of NOR R/S LATCH 14AA changing into LOW, and to cause the pulse of 10HZ not going thru NAND GATE 15AK, and simultaneously going thru the delay circuit comprising the INVERTER 14AB, SCHMITT TRIGGER 12AA, the lead-in wire 136 and OR GATE 12C to cause the "Q" terminal of NOR R/S LATCH 12D changing into LOW, and to cause the COUNTER 13AA stopping to count. The functions of NOR R/S LATCH 14AA and INVERTER 14AB are the same as that of NOR R/S LATCH 14AA and INVERTER 14AB are the same as that of NOR R/S LATCH 14A and INVERTER 14B.

7. When being connected with the time repeat station by dialing as shown in figure 6, a series of time repeat signals will, thru lead-in wire 99, enter into AND GATE 17A; the positive edge of each syllable square wave will go thru the differential circuit, and OR GATE 12C to cause the "Q" terminal of NOR R/S LATCH 12D changing to LOW; the pulse of 10HZ would not go thru AND GATE 12E and the COUNTER 13A will stop to count; the said differential signal will simultaneously go thru OR GATE 13B to cause the COUNTER 13A resetting.

The negative edge of each syllable square wave will go thru INVERTER 11A, the differential circuit and OR GATE 12B to have the "Q" terminal of NOR R/S LATCH 12D changing to HIGH, and the pulse of 10HZ will again go thru AND GATE 12E to enter into COUNTER 13A to start counting again, and repeat the same procedures.

As explained in (A) of (1) mentioned above, the Chinese type time repeat signal, "Du . . .", had a rather long silent interval from its front and rear syllables; it is separated from the front syllable with about 1.4 seconds of silent interval, and from its rear syllable with about 0.8 seconds of silent interval, and there is no other voice syllables having said longer silent interval from the front or the rear syllables; consequently, if any syllables having a silent interval with its front syllable over 1,4 seconds and with its rear syllable over 0.8 seconds, it must be the syllable of time repeat signal (Du . . .). In a series of syllable square waves A, B, C, if the silent interval between A and B is longer than 1.4 seconds, and the silent interval between B and C is shorter than 0.8 seconds, it indicates B being not a "Du . . . " signal.

When the negative edge of a A syllable square wave have the "Q" terminal of NOR R/S LATCH

12D changing to HIGH, and when a pulse of 10HZ going thru AND GATE 12E to enter into COUNTER 13A to count to 1.4 seconds, it will generate a pulse going thru AND GATE 16G to cause the "Q" terminal of NOR R/S LATCH 16H changing to HIGH; the positive edge of B syllable square wave will cause the COUNTER 13A resetting, and its negative edge will cause the COUNTER 13A re-counting to 0.1 seconds; then, it will generate a pulse going thru AND GATE 16A to cause the "Q" terminal of NOR R/S LATCH 16C changing to HIGH. Before the "Q" terminal of 16C changing to LOW, the C syllable square wave has been generated and will go thru AND GATE 16D and OR GATE 16E to cause the "Q" terminal of 16H changing to NOR, and to cause COUNTER 13A recounting. In a series of syllable square waves D, E, F, if the silent interval between D and E is longer than 1.4 seconds, and the silent interval between E and F is longer than 0.8 seconds, it indicates that E is the time repeat signal "Du . . . ", and the circuit will have the following results:

When the negative edge of syllable square wave D causing the "Q" terminal of NOR R/S LATCH 12D changing to HIGH, the pulse of 10HZ will go thru AND GATE 12E to cause COUNTER 13A starting to count; when the second pulse to 10HZ enters into COUNTER 13A (0.1 seconds), it will generate a pulse going thru AND GATE 16A to cause the "Q" terminal of NOR R/S LATCH 16C changing to HIGH; when the 9th pulse entering (0.8 seconds), COUNTER 13A will generate a pulse going thru OR GATE 16B to the "Q" terminal of NOR R/S LATCH 16C changing to LOW; when the 15th pulse entering (1.4 seconds), the COUNTER 13A will generate a pulse going thru AND GATE 16G to cause the "Q" terminal of NOR R/S LATCH 16H changing to HIGH. When next syllable square wave E appearing, its positive edge will cause the COUNTER 13A resetting, and its negative edge will cause the said COUNTER 13A re-counting; by the same token, when the second pulse of 10HZ entering (0.1 seconds), the "Q" terminal of NOR R/S LATCH 16C turning to HIGH; when the 9th pulse entering (0.8 seconds), COUNTER 13A will generate a pulse going thru OR GATE 16B and AND GATE 16I to cause the "Q" terminal of NOR R/S LATCH 16C changing to LOW, and "Q" terminals of 16J and 16L changing to HIGH; at this moment, the voice signal and time repeat signal will be separated by the HIGH and LOW voltages of "Q" terminal of 16L. When the 89th pulse entering (8.8 seconds), i.e., between the last syllable of voice signal and the "Du . . . " syllable of next time repeat signal, the COUNTER 13A will generate a pulse going thru OR GATE 16K to cause the "Q" terminal of NOR R/S LATCH 16L changing to LOW; when the "Q" terminal of 16L being HIGH, all signals appeared will be voice signal and will, thru AND GATE 18A, cause COUNTER 19A to count the number of syllable. When the "Q" terminal of 16L being LOW, the output of inverter 16M is in HIGH state; during the said interval, all the signal appeared are the time repeat signal, "Du . . .", which will go thru AND GATE 17A for output; the positive edge of said signal will cause COUNTER 13A resetting, and its negative edge will cause COUNTER 13A re-counting; so, the aforesaid procedures will be repeated every 10 seconds.

The calibration time of the embodiment No. 1 of this invention that is suitable for Chinese type of time repeat system is set at 04:00, or other time; its voice signal comprises 10 syllables, i.e., "hsia mien yin hsiang .szu dien ling fen ling miao". When the "Q" terminal of NOR R/S LATCH 16L being in HIGH state, the syllable counted by COUNTER 19A is ten, and the time repeat signal to be announced is that of 04:00, which will go thru AND GATE 20A and OR GATE 20C to cause the "Q" terminal of NOR R/S LATCH 21A changing to HIGH, and at the same time, the said HIGH will, thru lead-in wire 53, go to the "secondary timepiece". For the American type of time repeat system, just replace the dotted line portion 139A of figure 6 with dotted line portion 139B of figure 12 without changing other circuits. According to the explanation in (A), (2) of "1" above, the preparatory signal (Du) and time repeat signal (Lin) of the American type of time repeat system have longer silent interval for their adjacent syllables respectively; "Du . . ." has about 0.7 seconds silent interval from its front syllable, and has about 0.5 seconds silent interval from its rear "Lin . . ." syllable; the said "Lin . . ." syllable has about 1.4 seconds silent interval from its rear syllable, and there is no such conditions with other voice signal.

In a series of syllable square wave of G, H, I, J, if the silent interval between G and H is longer than 0.7 seconds, and the silent interval between H and I is shorter than 0.5 seconds; then the negative edge of G will let a pulse of 10HZ going thru lead-in wire 87 to cause COUNTER 13AA to count, and when the 8th pulse of 10HZ entering (0.7 seconds), COUNTER 13AA will generate a pulse going thru AND GATE 16AA to cause the "Q" terminal of NOR R/S LATCH 16AB changing to HIGH. When the syllable square wave appearing, its positive edge will have COUNTER 13AA resetting, and its negative edge will have COUNTER 13AA re-counting, after 0.1 seconds, it will generate a pulse going thru AND GATE 16AL to cause the "Q" terminal of NOR R/S LATCH 16AN changing to HIGH, and before the "Q" terminal of 16AN changing to LOW, the I syllable square has been generated; the said I will go thru lead-in wire 99, AND GATE 16A0 and OR GATE 16AF to cause the "Q" terminal of. 16AB changing to LOW, and to cause COUNTER 13AA re-counting. By the same token, if the silent interval between G and H is longer than 0.7 seconds, and the silent interval between H and I is longer than 0.5 seconds, and the silent interval between I and J is shorter than 1.4 seconds, and when the negative edge of G square wave makes COUNTER 13AA recounting for 0.7 seconds, the "Q" terminal of NOR R/S LATCH 16AB will change to HIGH, and when the negative edge of H

square wave makes the COUNTER 13AA counting for 0.5 seconds, the "Q" terminal of 16AD will change to HIGH as well; when the negative edge of I square wave has COUNTER 13AA counting for 0.1 seconds, the "Q" terminal of 16AN turns to HIGH. Before the "Q" terminal of 16AN changing to LOW, the J syllable square wave has been generated, and it will have the "Q" terminal of 16AB and 16AD changing to LOW, and have the COUNTER 13AA re-counting.

If the silent interval between H and I is longer than one second, COUNTER 13AA will, upon counting to one second, generate a pulse going thru AND GATE 16AE; then, the output of inverter 16AT is in HIGH state; consequently, the said pulse will go thru AND GATE 16AE and OR GATE 16AF to cause the "Q" terminals of 16AB and 16AD all changing to LOW so as to prevent the NOR R/S LATCH 16AI and 16AR from generating abnormal effect; for more details, see figure 12. In a series of syllable square waves of K, L, M, N, if the silent interval between K and L is longer than 0.7 seconds, and the silent interval between L and M is longer than 0.5 seconds, and between M and N is longer than 1.4 seconds; it indicates that L is the preparatory signal "Du . . .", and M is the time repeat signal "lin . . .", and the circuit will have the following results:

The negative edge of syllable square wave K will have the pulse of 10HZ entering into COUNTER 13AA thru lead-in wire 87 and causing the COUNTER 13AA to count. When the 8th pulse of 10HZ entering 0.7 seconds, COUNTER 13AA will generate a pulse going thru AND GATE 16AA to cause the "Q" terminal of NOR R/S LATCH 16AB changing to HIGH. When the syllable square wave L appearing, its positive edge will have the COUNTER 13AA resetting, and its negative edge will again have the COUNTER 13AA re-counting. When the 6th pulse of 10HZ entering (0.5 seconds), COUNTER 13AA again generates a pulse going thru AND GATE 16AC to cause the "Q" terminal of NOR R/S LATCH 16AD changing to HIGH; by the same token, the syllable square wave M will again have the COUNTER 13AA re-counting; when the 15th pulse of 10HZ entering (1.4 seconds), COUNTER 13AA will again generate a pulse going thru AND GATE 16AH to cause the "Q" terminals of NOR R/S LATCH 16AR changing to HIGH; beginning from this moment, the voice and time repeat (including preparatory) signals will be separated by the HIGH and LOW voltages of "Q" terminal of 16AR. When the 82nd pulse entering (8.1 seconds), which is approximately between the last syllable of voice signal and the next preparatory signal, "Du . . .", the COUNTER 13AA will again generate a pulse going thru OR GATE 16AQ to cause the "Q" terminal of 16AR changing to LOW. During HIGH state of "Q" terminal of 16AR, all the signals appeared are voice signal, going thru lead-in wire 99 and AND GATE 18AA to enter into the following circuit; during the LOW state of "Q" terminal of 16AR, inverter 16AS generates a HIGH output, and during that moment, the signal appeared is preparatory signal "Du . . ." and the time repeat signal "Lin . . .", which will go thru AND GATE 17A for output; the positive edge of said signal will have the COUNTER 13AA resetting, and its negative edge will have the COUNTER 13AA re-counting. The said procedures will repeat once again after every 10 seconds; for more details, see figures 6 and 12.

The embodiment No. 1 of this invention is suitable for the American type of time repeat system, and it is set at 04:10 AM, or other suitable time. According to the explanations in (B), (2) of "1" mentioned above, the voice signal comprises three syllable groups a, b, c, and the syllable groups a and b each have more than two syllables, while the syllable group b has two or more than two syllables before 04:00 and 50 seconds; at 04:01, the said b syllable group will reduce to only one syllable with longer silent intervals from its front and rear syllables; the said one syllable has a silent interval from its front syllable about longer than 0.5 seconds, and has a silent interval from its rear syllable about longer than 1.2 seconds; there is no other voice syllable having such long silent interval from its adjacent syllables; therefore, in a series of voice signal syllables, if there is any syllable having a silent interval from its front and rear syllables longer than 0.5 seconds and 1.2 seconds respectively, it must be the voice signal of 04:01, i.e. the only syllable group with one syllable.

In a series of voice syllable square waves of R, S, T which are going thru lead-in wire 99 and AND GATE 18AA for output, if the silent interval between R and S is longer than 0.5 seconds, and between S and T is shorter than 1.2 seconds; the S is not a one syllable signal. The negative edge of R square will go thru inverter 19AA and differential circuit to cause the "Q" terminal of NOR R/S LATCH 10AB changing to HIGH; the pulse of 10HZ will go thru lead-in wire 71 and AND GATE 19AC to cause counter 19AE starting to count. When the 6th pulse of 10HZ entering (0.5 seconds), counter 19AE will generate a pulse to cause the "Q" terminal of NOR R/S LATCH 19AG changing to HIGH; if the silent interval between R and S syllables is over 1.2 seconds, the "Q" terminal of NOR R/S LATCH 19AL is in LOW state, and the output pulse of counter 19AE would not go thru AND GATE 19AH, and the "Q" terminal of NOR R/S LATCH 10AI would not change its existing state. When syllable square wave S appearing, its positive edge goes thru the differential circuit and OR GATE 19AD to cause the counter 19AE resetting, and to cause the "Q" terminal of NOR R/S LATCH 19AB changing to LOW, and the pulse of 10HZ would not go thru AND GATE 10AC; the negative edge of said pulse makes counter 19AE re-counting, and upon counting for 0.1 seconds, the said counter will generate a pulse going thru AND GATE 19AJ to cause the "Q" terminal of NOR R/S LATCH 19AL changing to HIGH. Before the "Q" terminal of 19AL changing to LOW, the said syllable square wave T has been generated, will go thru AND

GATE 19AM and OR GATE 19AF to cause the "Q" terminal of 19AG changing to LOW, and to cause the counter 19AE re-counting; for more details see figure 12.

In a series of voice syllable square waves of U, V, W, if the silent interval between U and V is longer than 0.5 seconds, and between V and W is longer than 1.2 seconds; in that case, the V is the only syllable "one" of syllable group "b" of voice signal at 04:01; then, the circuit will have the following results; The negative edge of syllable wave U makes the counter 19AE to count, and upon counting for 0.5 seconds, the said counter will generate a pulse to cause the "Q" terminal of 19AG changing to HIGH. Upon syllable square wave V appearing, its positive edge causes counter 19AE resetting, and its negative edge will cause 19AE re-counting for 0.1 seconds; then, it will generate a pulse going thru AND GATE 19AJ to cause the "Q" terminal of 10AL changing to HIGH, which will be sent to AND GATE 19AH. Upon counting for 1.2 seconds, 19AE will again generate a pulse going thru AND GATE 19AH to cause the "Q" terminal of 10AI changing to HIGH, which will further be sent to AND GATE 20AD. When inverter 16AS generating a HIGH and going thru lead-in wire 135 and entering into AND GATE 17A, the syllable square wave of preparatory signal "Du . . ." and the time repeat signal "Lin . . ." will go thru lead-in wire 99, AND GATE 17A and lead-in wire 134 to enter into inverter 20AA and AND GATE 20AD. The negative edge of square wave of the preparatory signal "Du . . ." goes thru inverter 20AA, and the differential circuit to cause the "Q" terminal of NOR R/S LATCH 20AC changing to HIGH: therefore, only the square wave of time repeat signal "Lin . . ." appeared afterwards can go thru AND GATE 20AD; now, the said square wave of "Lin . . ." is the time repeat signal right at 04:01, which will then go thru lead-in wire 132 and OR GATE 20C to cause the "Q" terminal of NOR R/S LATCH 21a changing to HIGH, and at the same time, it will go thru lead-in wire 53 to enter into the secondary timepiece; see figures 6 and 12 for further details.

8. As explained in "4" mentioned above, a pulse of 1 HZ goes thru lead-in wire 76 to cause counter 24A counting at constant speed and in synchronization with timepiece 41; when counting to the designed calibration time (04:00 of Chinese type, or 04:01 of American type), it will generate a pulse to cause the "Q" terminal of NOR R/S LATCH 25A changing to HIGH; for further details, see figure 6.

9. As shown in figures 5, 6 and 7, if the "Q" terminal of NOR R/S LATCH 21A being HIGH first, and as soon as the "Q" terminal of NOR R/S LATCH 25A changed to HIGH, the output of "Q" terminal of 21A will go thru lead-in wire 79 to cause inverter 27A sending a LOW to AND GATE 27B. When the HIGH pulse of "Q" terminal of 25A entering 27B thru lead-in wire 92, the "Q" terminal of NOR R/S LATCH 27C is still in LOW state. However, when the "Q" terminal of 25A changing to HIGH, it will cause the "Q" terminal of 27C changing to HIGH simultaneously.

10. As shown in figures 5, 6 and 7, when the "Q" terminal of NOR R/S LATCH 21A or 25A changing to HIGH, which goes thru OR GATE 28D to enter into AND GATE 28E, a pulse of 10HZ will go thru lead-in wire 71, AND GATE 23B and 28E to enter into counter 28I, 28J and 28K for counting the time difference, and the OR GATE 280 changes its output to HIGH. When the "Q" terminal of 21A and 25A changing to HIGH, the output of AND GATE 28A will be a HIGH, going thru inverter 28B to become a LOW entering into AND GATE 28E; at this moment, the counter 28I, 28J, 28K stop to count, and at the same time, the 10HZ pulse will go thru AND GATE 28C to enter into counter 28F, 28G, 28H for counting, and when their counting is equal to the time difference counted by counter 28I, 28J, 28K, the output of OR GATE 280 changes to LOW, and the counter 28F, 28G, 28H stop to count.

11. If the "Q" terminal of NOR R/S LATCH 21A changing to HIGH is earlier than the "Q" terminal of 25A changing to HIGH, the "Q" terminal of NOR R/S LATCH 27C will be in LOW state in accordance with the explanation in "9" mentioned above; then, the inverter 27D generates a HIGH, going thru OR GATE 30A to enter into AND GATE 30B; consequently, when the telephone time repeat signal designed makes the "Q" terminal of 21A changing to HIGH, the said HIGH pulse will go thru lead-in wire 79, AND GATE 30B, and the differential circuit, from which a differential signal is generated and going thru lead-in wire 65 to enter into the timepiece 41 for resetting the seconds to zero; at the same time, the HIGH of the "Q" terminal of 21A will go thru AND GATE 31A and lead-in wire 66 to enter into the timepiece 41 to cause the "fast set control" working until the timepiece 41 running to the time calibration moment designed, i.e. 04:00 (In American type, it is 04:01), and then it will generate an excitation signal going thru lead-in wire 120 and AND GATE 1M to cause the "Q" terminal of NOR R/S LATCH 1J changing to LOW, which will then go thru lead-in wire 84 and AND GATE 31A to stop the "fast set control" and to continue the counting; now, the time indicated by timepiece 41 is the standard time, i.e., 04:00 (In American type, it will be 04:01). Up to this moment, to calibrate the timepiece lagging the standard time is automatically done. However, the "Q" terminal of 25A changing to HIGH is earlier than the "Q" terminal of 21A changing to HIGH, the "Q" terminal of 27C will be in HIGH state in accordance with the explanations in "9" mentioned above. According to the explanations in "10" mentioned above, when the timepiece 41 reaches 04:00, the time of calibration designed (In American type, it is 04:01), it will generate a pulse to cause the "Q" terminal of 25A changing to HIGH, and to cause the counter 28I, 28J, 28K counting the time difference, and also to cause OR GATE 280 generating a HIGH to enter into AND GATE 29A; consequently, when the "Q"

terminal of 21A changing to HIGH, the said HIGH will go thru lead-in wire 79, AND GATE 29A, and lead-in wire 64 to enter into timepiece 41 and to stop the timepiece for an interval which is equal to the time difference; in other words, the timepiece resumes to run upon the output of OR GATE 280 changing to LOW; then, the time indicated by the timepiece 41 is the standard time, and to calibrate the timepiece ahead of standard time is automatically done; for further details, see figures 2, 4, 5, 6 and 7. If the conventional timepiece is a hand type timepiece, the dotted line portion 138A of figure 7 should be replaced with the dotted line portion 138B of figure 9. If the "Q" terminal of NOR R/S LATCH 21A changing to HIGH is earlier than the "Q" terminal of 25 A changing to HIGH, the pulse of 240 HZ will enter into divider 37B thru lead-in wire 74 and will be divided by 10; then, the pulse of 24HZ will go thru AND GATE 37A and lead-in wire 66 to enter into timepiece 41 to have the second hand of timepiece rotating fast; when the second hand reaching to the calibration time designed, 04:00 (In American type, it is 04:01), the "Q" terminal of NOR R/S LATCH 10Q changes to LOW as explained in "3" above; then, the said LOW pulse goes thru lead-in wire 84 to enter into AND GATE 37A to stop the fast rotating of second hand and to continue counting time. Now, the time indicated by the timepiece 41 is the standard time of 04:00 (In American type, it is 04:01), and to calibrate the timepiece lagging the standard time is done automatically. On the contrary, if the "Q" terminal of 25A changing to HIGH is earlier than the "Q" terminal of 21A changing to HIGH, the output of AND GATE 36A will go thru lead-in wire 64 entering into timepiece 41 to stop the timepiece for an interval which is equal to the time difference; then, the time indicated by the timepiece is the standard time, and the calibration of timepiece ahead of standard time is done automatically. The theory of generating stopping signal with AND GATE 36A is the same as that of AND GATE 29A; for further details, see figures 5, 6, 7, 8 and 9.

12. If the timepiece 41 is lagging the standard time, the NOR R/S LATCH 27C will, in accordance with the explanation in "9" mentioned above, remain its "Q" terminal in LOW, and the pulse of 10HZ will go from AND GATE 28C, and thru AND GATE 32A and lead-in wire 67 for further output; on the contrary, if the timepiece 41 is ahead of the standard time, the time difference pulse of 10HZ will go thru AND GATE 33A and lead-in wire 68 for further output. According to the explanation in "10" mentioned above, the number of output pulse will be just equal to the time difference number counted by counter 28I, 28J, 28K, and each pulse is equal to 1/10 seconds of time difference as shown in figures 2 and 7.

For the timepiece 41 having any calibration device there is switch 44 being connected to "+V"; if the said timepiece is lagging the standard time, the time difference pulse will go thru AND GATE 32A, OR GATE 34A to enter into divider 34A and to be divided by 1; then, the time difference pulse of 1HZ will go thru AND GATE 34D, lead-in wire 94, OR GATE 4K and AND GATE 4M to enter into counter 4W for memory. By the same token, if the timepiece 41 is ahead of standard time, the time difference pulse will go thru AND GATE 33A, OR GATE 34A to enter into divider 34B and to be divided by 10; then, the time difference pulse of 1HZ will go thru AND GATE 34C and lead-in wire 89 to enter into counter 4Z and 4ZA for remembering the time difference of timepiece 41 so as to use the said memory for resetting the time of dialing the telephone of time repeat station; the theory of circuit function is the same as that explained in "5" mentioned above as shown in figures 2, 5, 7. If the timepiece 41 having calibration device, the switch 44 will be connected to ground; if the timepiece 41 is lagging the standard time, the time difference pulse of 10HZ will be generated from AND GATE 32A, going thru lead-in 67 to enter into the fast setting device of timepiece 41 so as to automatically calibrate the timepiece lagging the standard time. By the same token, if the timepiece 41 is ahead of the standard time, the time difference pulse of 10HZ will be generated by AND GATE 33A, going thru lead-in wire 68 to enter into the backward setting device of timepiece 41 so as to automatically calibrate the timepiece ahead of the standard time as shown in figures 2 and 7.

13. If the telephone time repeat signal has set the "Q" terminal of NOR R/S LATCH 21A in HIGH, the said HIGH will go thru lead-in wire 79 the retarding circuit, and OR GATE 5E to cause the "Q" terminal of NOR R/S LATCH 5D changing to LOW; then, the telephone line 46 will be separated from the coupling transformer 8A, and connected with telephone set 40 as shown in figures 4, 6 and 10.

14. As explained, in "10" mentioned above, when counter 28F, 28G, 28H count to a number which is equivalent to the time difference recorded by counter 28I, 28J, 28K, the output of OR GATE 28O is LOW, and the output of inverter 28P is HIGH, which will go thru the retarding circuit comprising AND GATE 28Q, OR GATE 35B, and SCHMITT TRIGGER 35A, and the differential circuit, the lead-in wire 75, and OR GATE 1K, and OR GATE 1C and 1H to cause the "Q" terminals of NOR R/S LATCH 1B and 1I changing to LOW; then, all circuits will be recovered to the state as explained in "2" mentioned above as shown in figures 4 and 7.

15. For the timepiece using A.C. power, in case of the power being off and turning on again, the SCHMITT TRIGGER 26D will generate an excitation signal to cause the "Q" terminal of NOR R/S LATCH 26E changing to HIGH, and the circuit will have the following results:

(A) The said HIGH will go thru OR GATE 26F and 26I to acuse the "Q" terminal of NOR R/S LATCH 26H changing to LOW, and the "Q" terminal of 26K changing to HIGH; then, the rest

circuits will be restored to the state as explained in "2" mentioned above as shown in figure 7.

(B) The said HIGH will go thru lead-in wire 70 and OR GATE 2D to cause the OSC. composed with SCHMITT TRIGGER 2E generating a pulse of 10HZ, which will go thru inverter 2F, lead-in wire 71 and AND GATE 26A to cause the LED 26B to flash to show the power being off as shown in figures 4 and 7.

(C) The "Q" terminal of NOR R/S LATCH 26K will change to HIGH which will go thru lead-in wire 86 to enter into AND GATE 4B and 4C; then, the starting time of next dialing the time repeat station will be advanced to 03:58 and one second (It may set at other time), and the counter 24A will generate a pulse, going thru AND GATE 4B and 4C for exciting the following circuits as shown in figures 5 and 7.

(D) The time difference counted by counter 28I, 28J, 28K at the first time calibration after the power being on should be considered as not the time difference of a whole day; now, the "Q" terminal of NOR R/S LATCH 26H changes to LOW, and the time difference pulse at this time will not go thru AND GATE 32A or 33A for output as shown in figure 7.

(E) Upon the completion of the first time calibration after the power being on, the "Q" terminal of NOR R/S LATCH 26H will be restored to HIGH, and the "Q" terminal of 26K will again restored to LOW upon the completion of second time calibration as shown in figure 7.

16. In case of the telephone being interrupted during the circuit being functioning, AND GATE 26F, or let counter 24A generate, at 04:02 (It may be set at other time), a pulse, going thru lead-in wire 88 to enter into OR GATE 26F for generating the circuit function as explained in (A), (C), (D), (E) of "15" mentioned above; for further details, see figures 5, 6, 7.

17. Under normal condition, the switch 43 is connected to "+V" 56; in case of power being off for over 25 minutes, or the timepiece having a time difference for over 25 minutes, the switch 43 may be connected to ground; then, the circuit will automatically dial the telephone time repeat station, and the time repeat voice and signal will be announced by speaker 9B for time calibration. When the switch 43 being connected to ground, the output of SCHMITT TRIGGER 38A is HIGH, which will go thru lead-in wire 51 to cause the "Q" terminal of NOR R/S LATCH 26E changing to LOW, and stop the LED 26B flashing as shown in figures 4, 7, 10.

18. In case of calibrating the time and re-setting the speed once a day, the switch 42 should be connected to the ground; the case of the said switch 42 being connected to "+4" 56, the time calibration and the speed resetting will be once every hour. Under such condition, the counter 24A will, at about 10 seconds (In American type, it is at the first minute and zero second of each hour), generate a pulse, which will go thru AND GATE 4D and 4E to excite the automatic dialing circuit as shown in figures 4 and 5.

For time difference counting, the OSC. circuit composed with SCHMITT TRIGGER 2H will generate a pulse of 240 HZ, which will go thru inverter 2G, lead-in wire 74, AND GATE 23A, OR GATE 23C, and AND GATE 23A, or GATE 23C, and AND GATE 28E to enter into counter 28I, 28J, 28K for fulfilling the said function as shown in figure 7. In the embodiment No. 1 of this invention, the secondary timepiece system comprises only 1—3, 9, 21, 23—33, 35—39, 43, 55 and the conventional timepiece 114 as shown in figures 2 and 11, and the theory of circuit functions is the same as that the primary timepiece mentioned above.

Claims

1. A timepiece comprising means for periodically and automatically connecting the timepiece to a standard time signal via a telephone system and means for automatically synchronising the timepiece with the standard time signal.

2. A timepiece as claimed in claim 1, comprising means for automatically adjusting the frequency of the timepiece subsequent to connection to the standard time signal and in correspondence with the deviation of the timepiece from ths standard time.

3. A method of automatically maintaining the accuracy of a timepiece comprising periodic and automatic connection to a standard time signal via a telephone system and automatic synchronisation with the standard time signal.

4. A method as claimed in claim 3, further comprising automatically adjusting the frequency of the timepiece subsequent to connection to the standard time signal and in correspondence with the deviation of the timepiece from the standard time.

5. A timepiece with automatic time setting system through dial telephone line and automatic speed adjusting system comprising: the automatic dial circuit, the separating circuit of time repeat signal and voice signal, the discrimination circuit of voice signal and the analysing circuit of time signal designed for time calibration, the synchronising time count circuit of timepiece, the synthetic circuit of time differential signal, the telephone line switching circuit and the automatic adjusting circuit of dialing starting time, and the conventional digit or hand type timepiece and forming the primary timepiece; and then it being connected through the telephone line, to several secondary timepieces which being in simple structure; and through the circuit connection among these timepieces, a standard time to be calibrated by these timepieces simultaneously and their speed to be adjusted respectively and dialing starting time to be set automatically as well.

6. A timepiece and its related system as claimed in claim 5, wherein a conventional timepiece will start the operation of this invention

by turning on the synchronising circuit of timepiece to count the time with a constant speed, and by activating the said automatic dialing circuit for connecting telephone line and through its time difference stored in the memory circuit a non-periodical output signal will trigger the automatic dial circuit to call through telephone line to the time repeat station before announcing the standard time of calibration.

7. A synchronising time count circuit of timepiece as claimed in claim 5, which can, with a constant speed count time in synchronizing state with the timepiece so as to trigger the time calibration signal for comparing the time difference with that of time repeat station on the telephone line.

8. A separating circuit of time repeat signal and voice signal and a discrimination circuit of voice signal and an analysing circuit of time signal designed for time calibration as claimed in claim 5, which will count the silent intervals between the said adjacent syllables and the number of syllables of the signals on telephone line, and will analyse and pick up the time repeat signal designed for time calibration so as to force the primary and secondary timepieces simultaneously and automatically calibrating the standard time with the announcement of time repeat station.

9. A synthetic circuit of time differential signal as claimed in claim 5, which will generate a corresponding time differential signal to compel the primary and the secondary timepieces automatically adjusting their speed respectively.

10. A telephone line switching circuit and an automatic adjusting circuit of dialing starting time as claimed in claim 5, which will put the time differential signal in memory circuit to automatically trigger the automatic dial circuit for connecting the time repeat station in due time.

11. A system of synchronised timepieces including a timepiece as claimed in claim 1 or claim 2.

12. A timepiece substantially as hereinbefore described with reference to and as illustrated in the accompanying drawings.

13. A method of automatically maintaining the accuracy of a timepiece substantially as hereinbefore described and illustrated by reference to the accompanying drawings.

Printed for Her Majesty's Stationery Office by the Courier Press, Leamington Spa, 1983. Published by the Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.